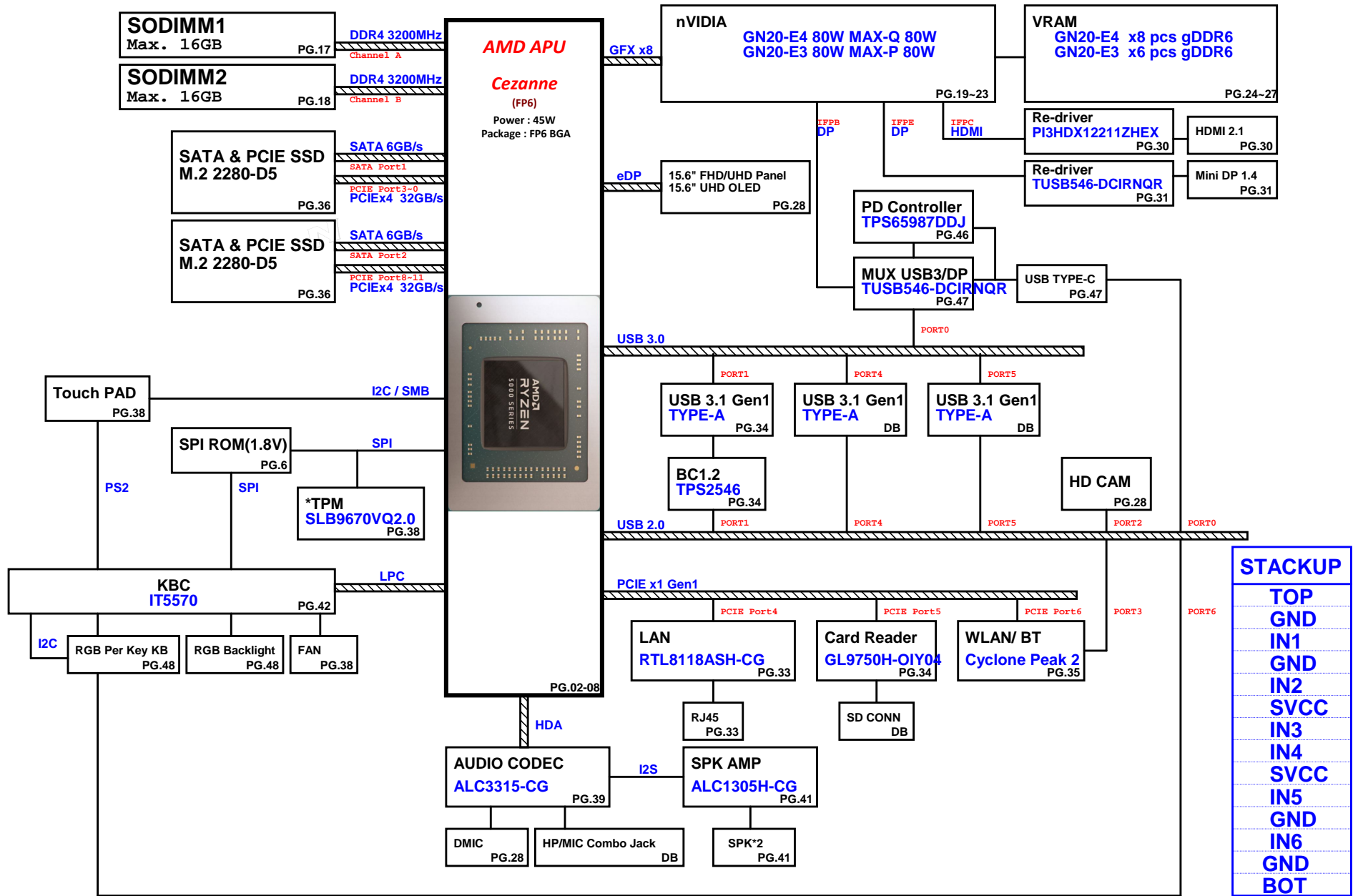


Valkyrie AMD Cezanne & NV G20E



PCIe Port	Function
GFX 0~8	GPU
PCIe 3~0	SSD1(PCIe/SATA)
PCIe 4	LAN
PCIe 5	CARD Reader
PCIe 6	WLAN
PCIe 7	NC
PCIe 8~11	SSD2(PCIe/SATA)

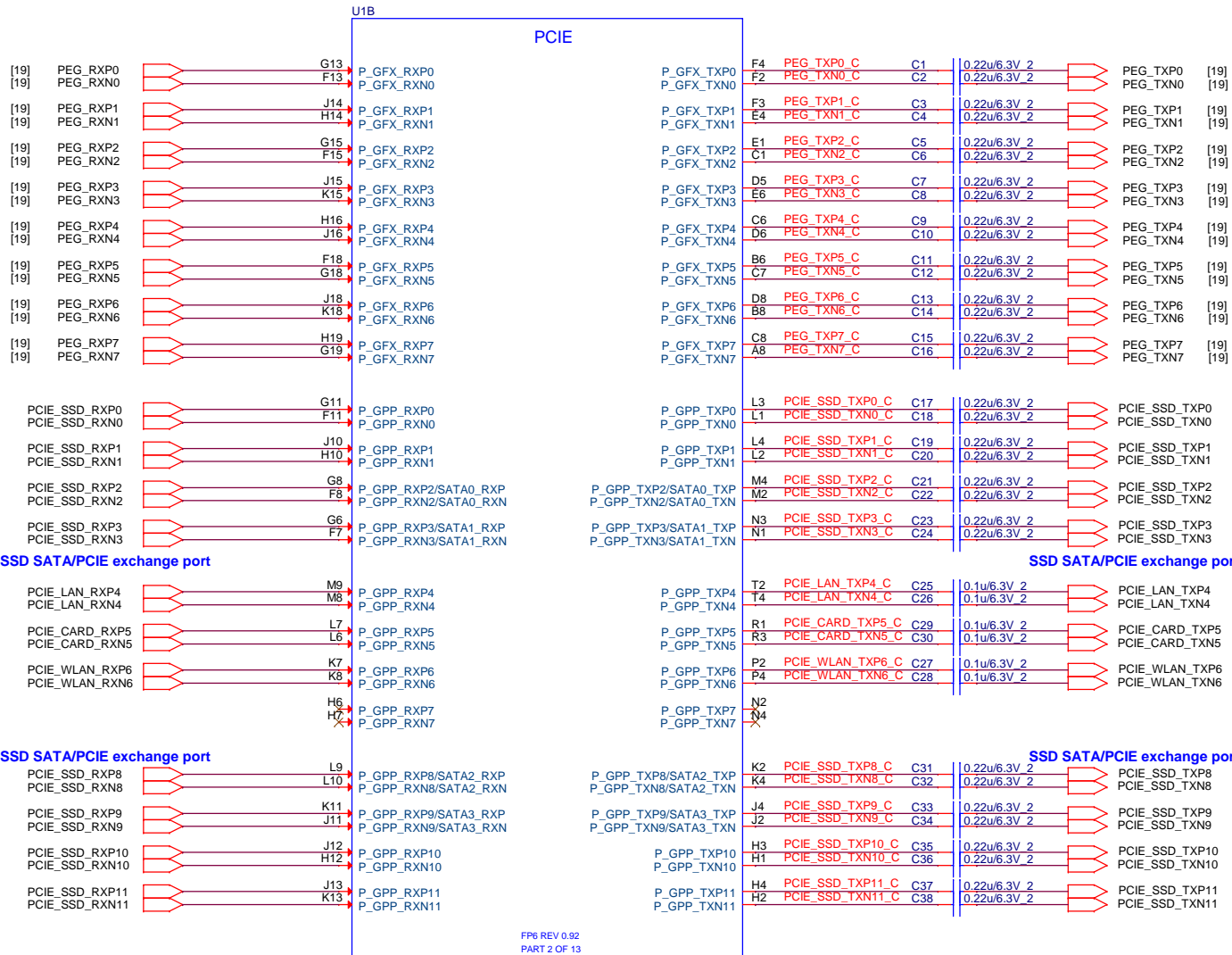
PCIe-SSD 4 lane
(Port3 --> Port0)

LAN


CARD

WLAN

PCIe-SSD 4 lane
(Port8 --> Port11)

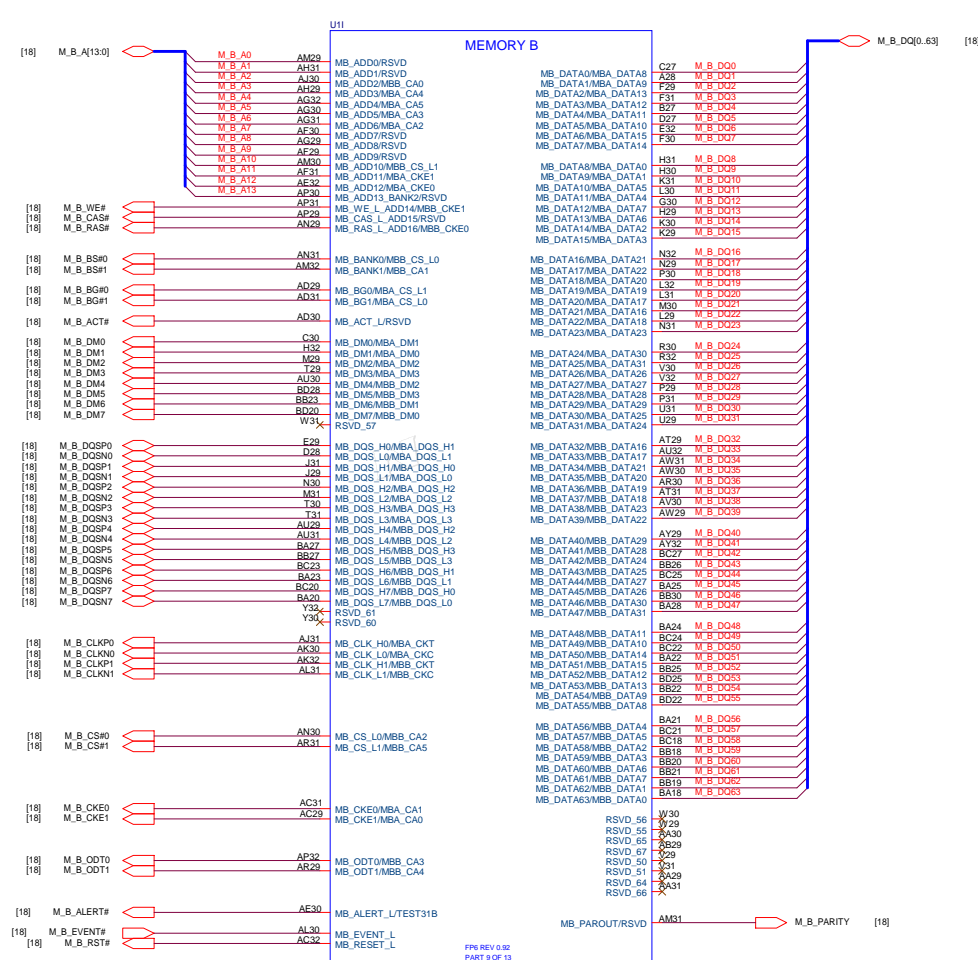


AMD APU	Quanta Description	Quanta PN	Stage
TBD	CPU(1140P)100-000000300-30 1.6G-8C(BGA)	AJ00100VT06	DB

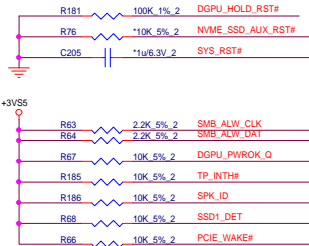
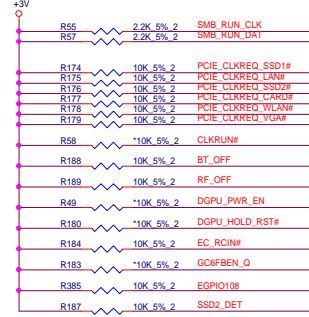
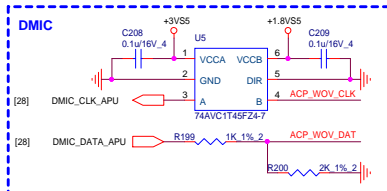
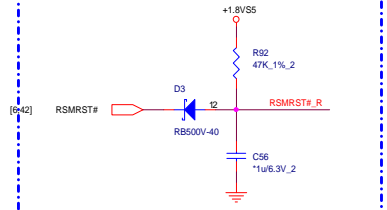


PROJECT : G3EF
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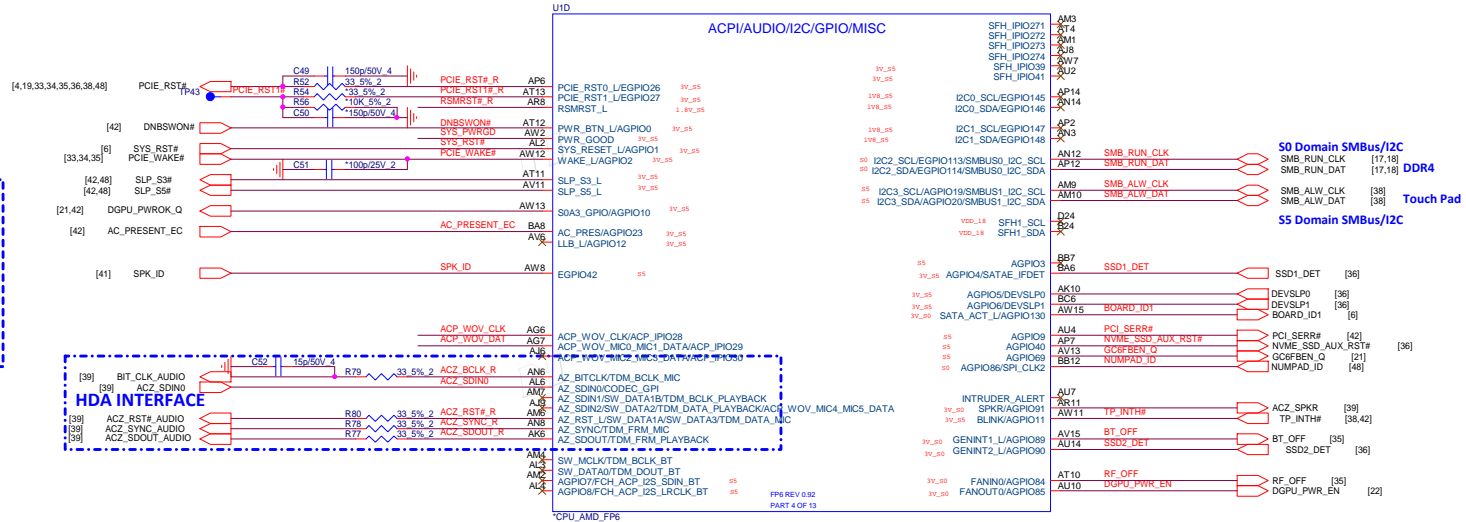
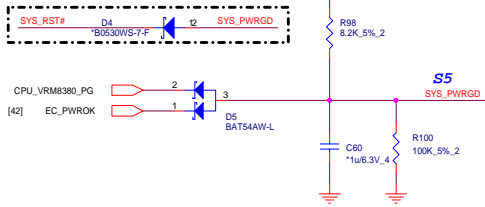
Size Custom	Document Number Cezanne 1/7(PCIe)	Rev 1A
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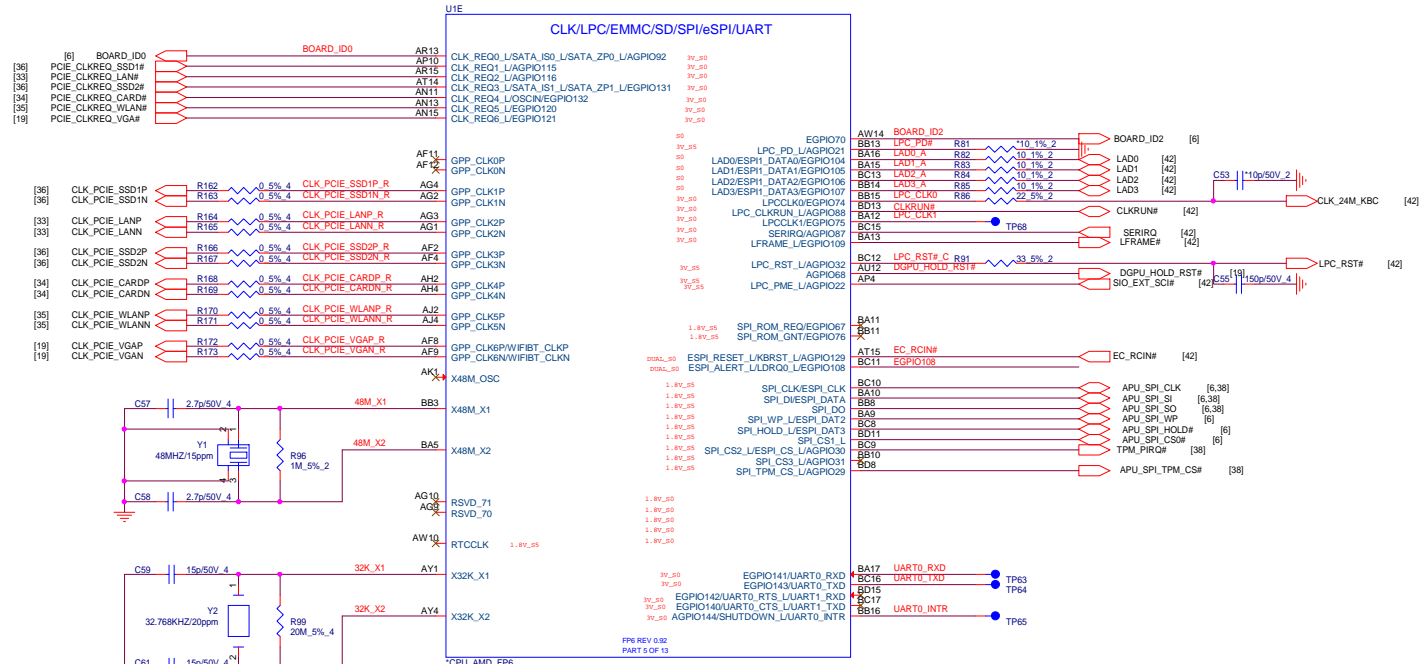

```
-----RSMRST_GATE# from EC
```



PWRGD CIRCUIT



NVME_SSD_AUX_RST# & LPC_PD#
If unused, enable internal pull up or pull down by software.



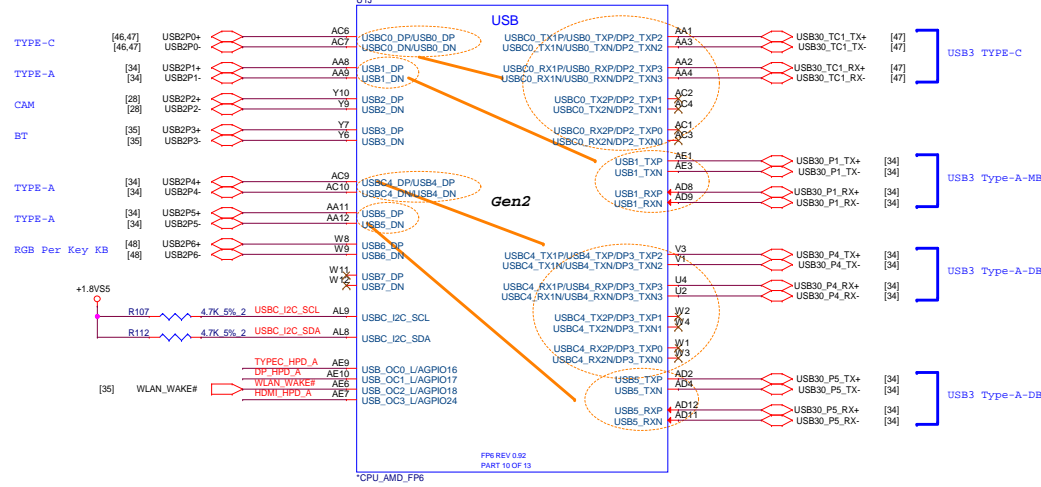


BOARD ID SETTING



BOARD_ID0	BOARD_ID1	BOARD_ID2	Definition
0	0	0	GN20E - E4
0	0	1	GN20E - E3
0	1	0	Reserved
0	1	1	Reserved

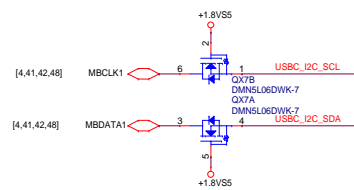
USB3 and USB2 Port Mapping



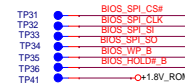
USB2 Port	Function
USB0	TYPE-C
USB1	TYPE-A
USB2	CAM
USB3	BT
USB4	TYPE-A
USB5	TYPE-A
USB6	RGB Per Key KB
USB7	NC

USB3 Port	Function
USB0	TYPE-C
USB1	TYPE-A-MB
USB4	TYPE-A-DB
USB5	TYPE-A-DB

G3HA add USB_C_I2C circuit for measure



TP(TP2675) need place to the same layer



ROM (No support RPMC)

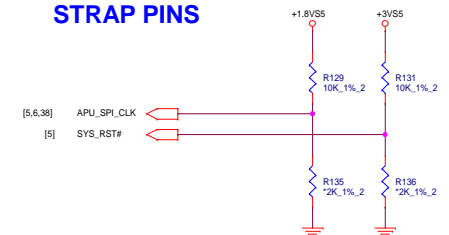
MV stuff SOP8 BIOS ROM only

Vender	Size	P/N (1.8V)
WND	1.6M	AKE5DZNON01 W25Q128FWSIF
GGD	1.6M	AKE5DZNOQ02 GD25LQ128DSIGR
Socket	DG008000011	

DB & SI & PV stuff WSON8 SOCKETwith BIOS ROM

Vender	Size	P/N (1.8V)
WND	1.6M	AKE5DFNKN01 W25Q128FWPIF
GGD	1.6M	AKE5DZNKQ01 GD25LQ128DWIGR
Socket	DG008000012	

STRAP PINS

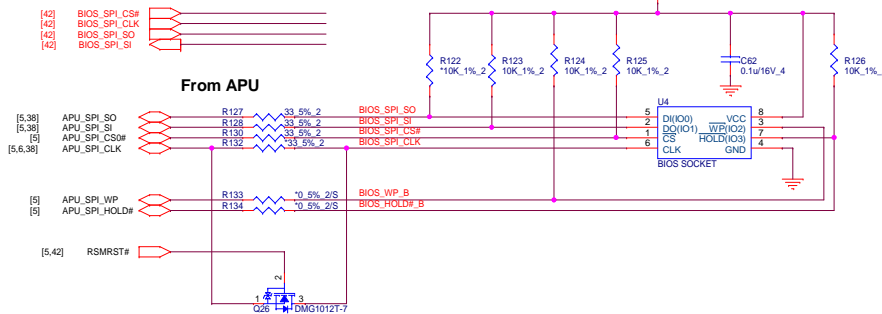


REQUIRED STRAPS

	APU_SPI_CLK	SYS_RST#
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks	Normal reset mode
PULL LOW	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	Short reset mode

From EC

From APU



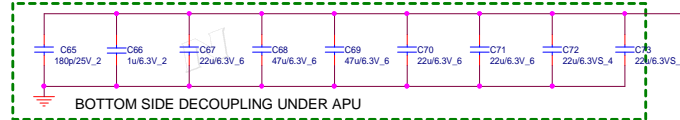
Vgs should be less than 1.5V



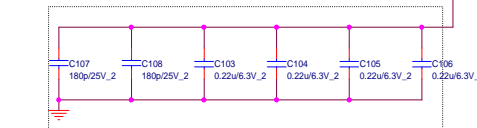
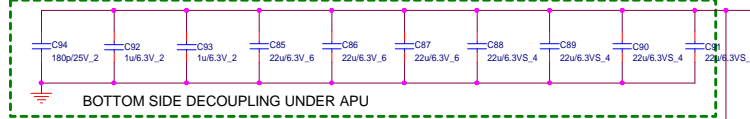
PROJECT : G3EF
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Check list VDDCR_SOC: 7*22UF+1*1U+1*180PF

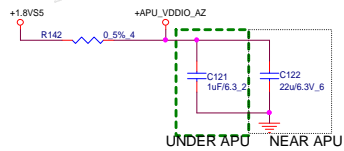


Check list VDDCR_SOC: 7*22UF+2*1UF+4*0.22uf+3*180PF

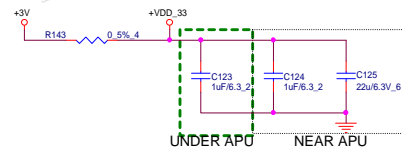


Decoupling between process and DIMMs across VDDIO and VSS split.

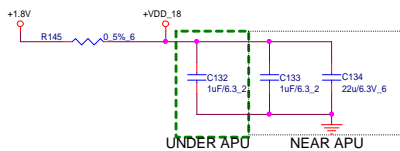
Check list VDDIO_AUDIO: 1*22UF+1*1UF



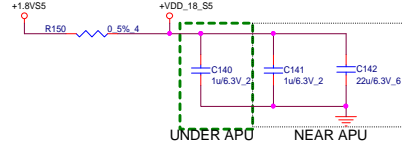
Check list VDD_33: 1*22UF+2*1UF



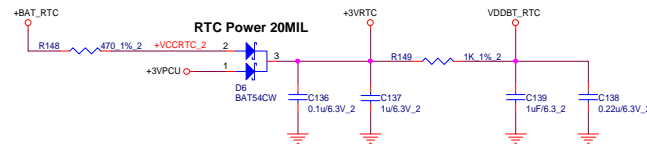
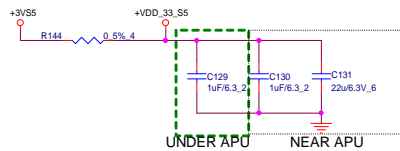
Check list VDD_18: 1*22UF+2*1UF



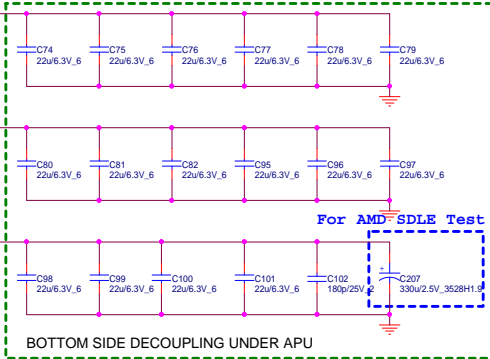
Check list VDD_18_S5: 1*22UF+2*1UF



Check list VDD_33_S5: 1*22UF+2*1UF



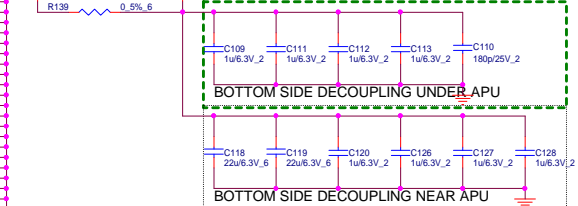
Check list VDDCR: 16*22UF+1*180PF



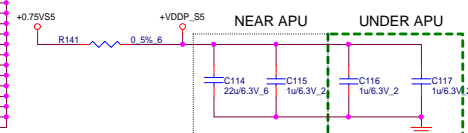
For AMD SDLE Test

BOTTOM SIDE DECOUPLING UNDER APU

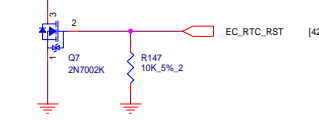
Check list VDDP: 2*22UF+8*1UF+1*180PF

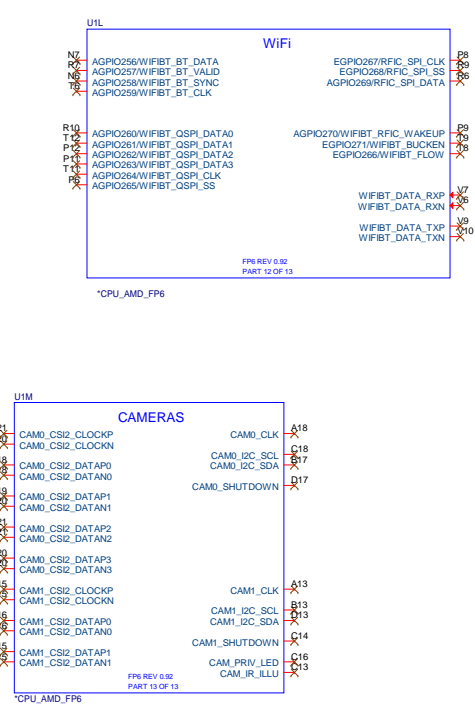
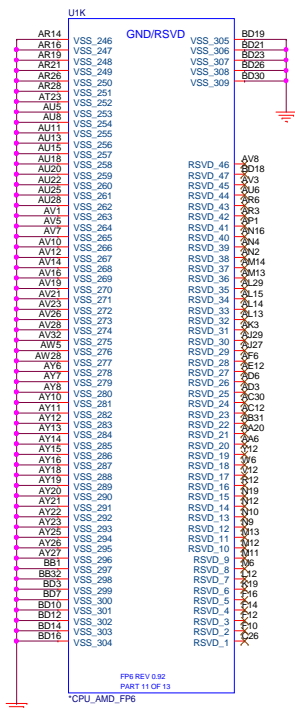
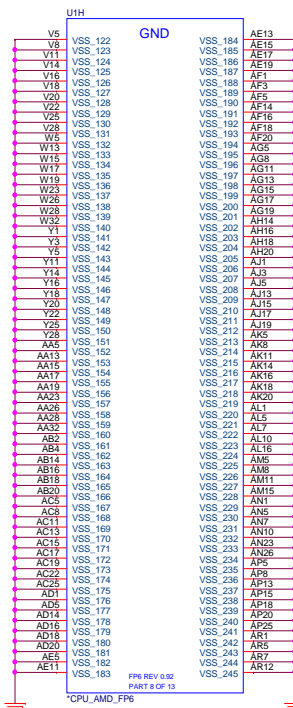
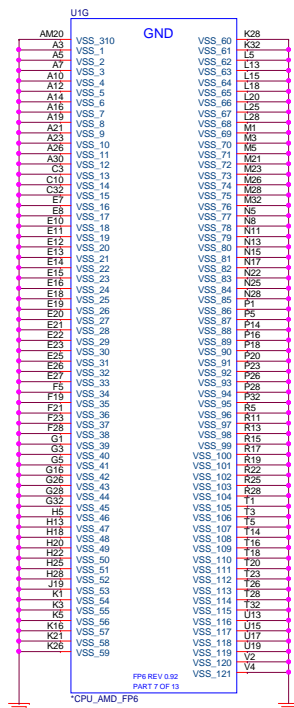


Check list VDDP_S5: 1*22UF+3*1UF




EC RTC RESET





09

NA




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Quanta Computer Inc.

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Quanta Computer Inc.

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Quanta Computer Inc.

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PROJECT : G3EF

Quanta Computer Inc.

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NA



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Quanta Computer Inc.

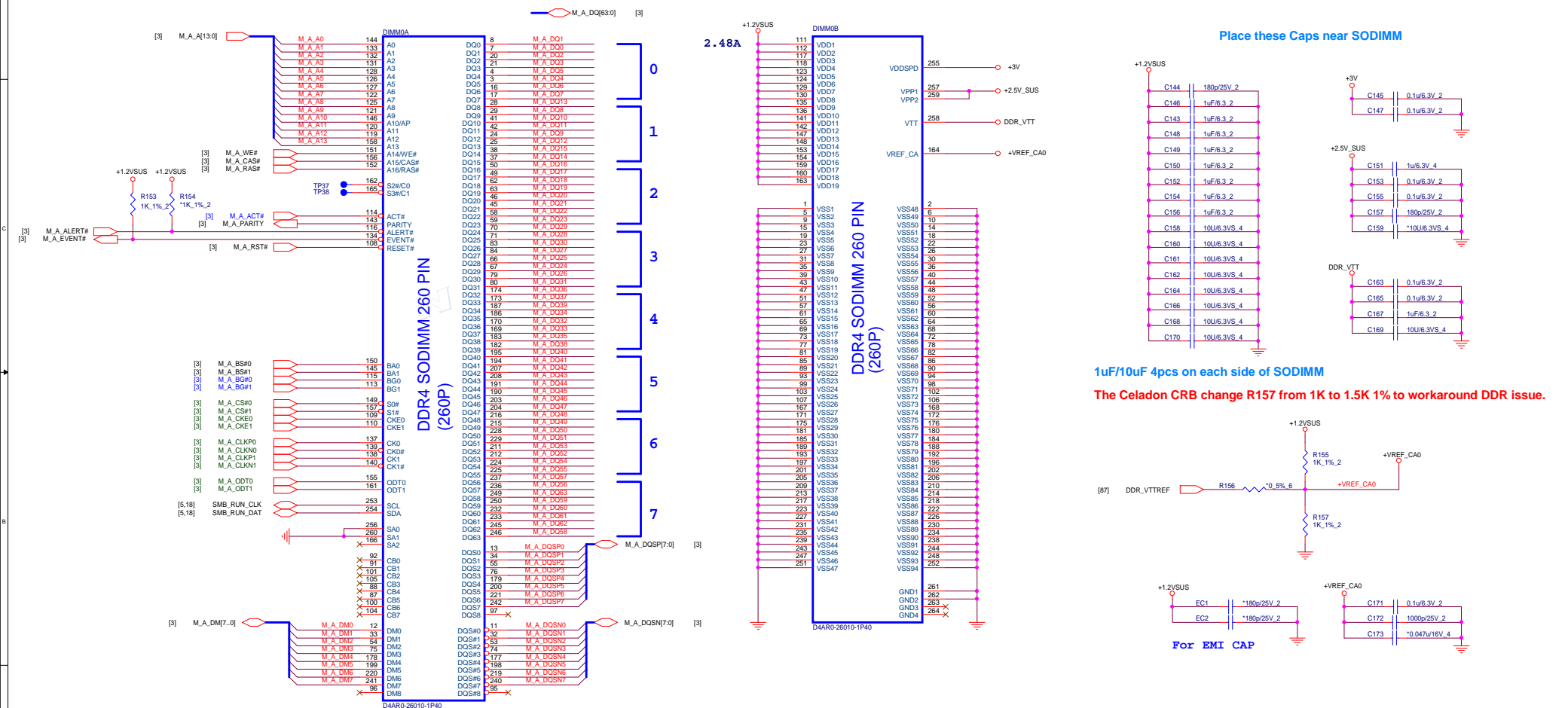
Size A	Document Number PCH(NA)	Rev 1A
Date: Thursday, October 08, 2020		Sheet 5 of 106

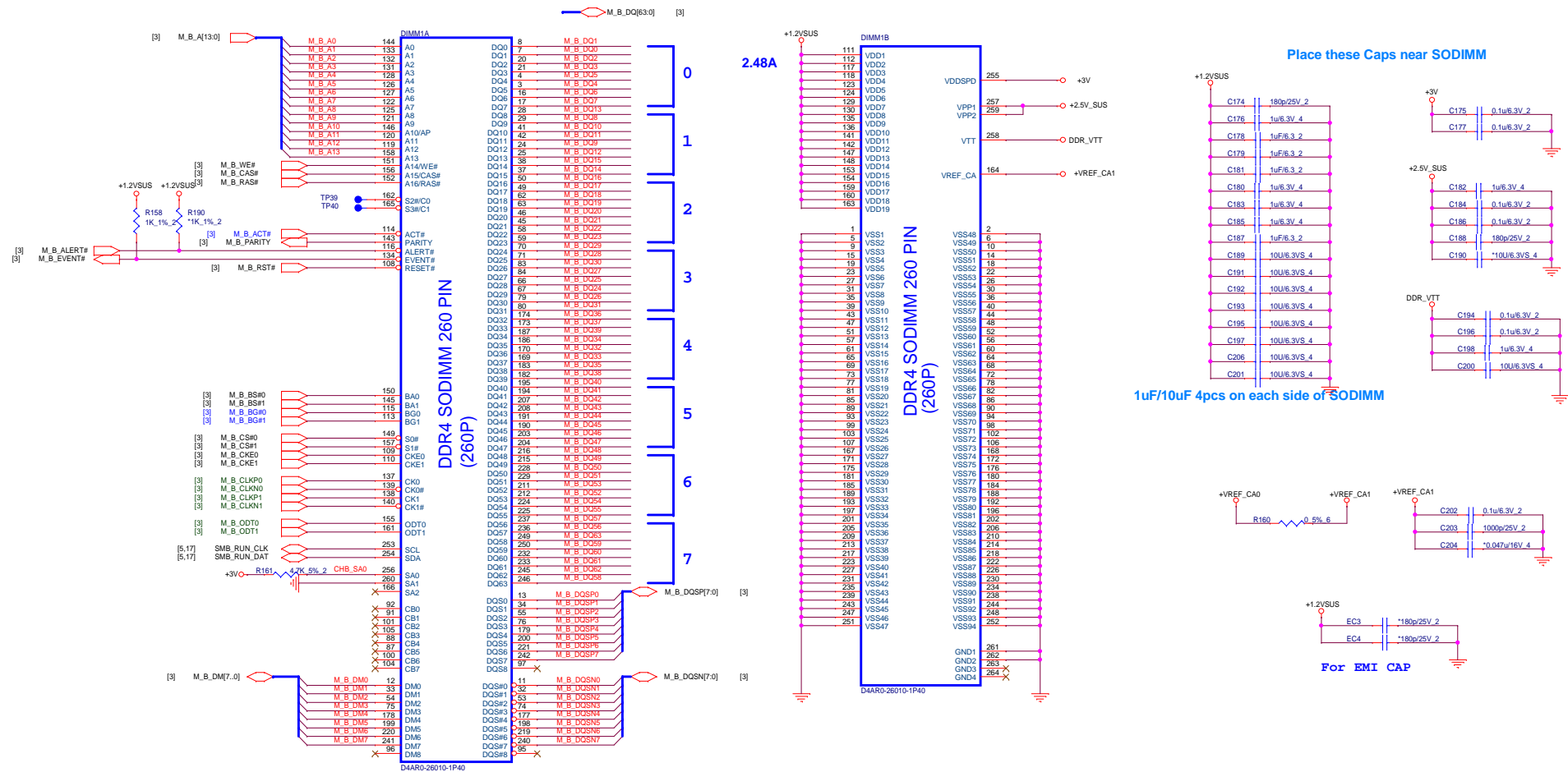
NA

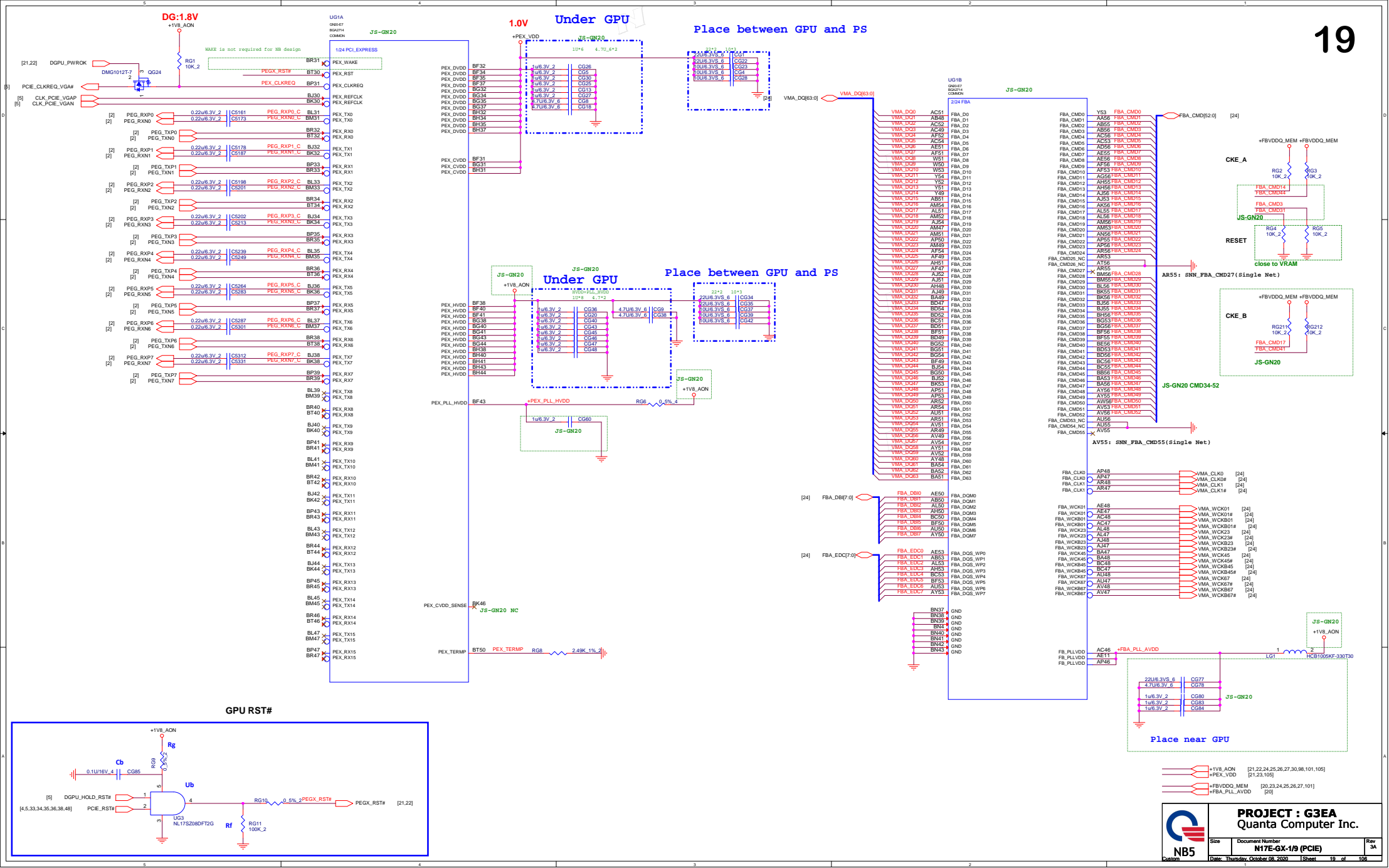


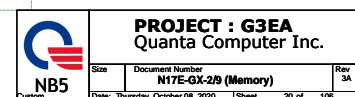
PROJECT : G3EF
Quanta Computer Inc.

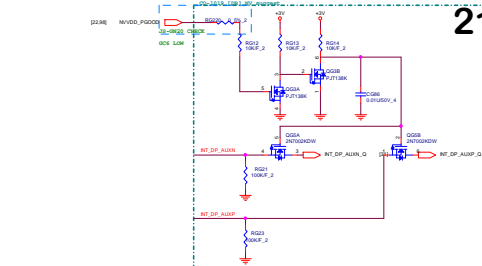
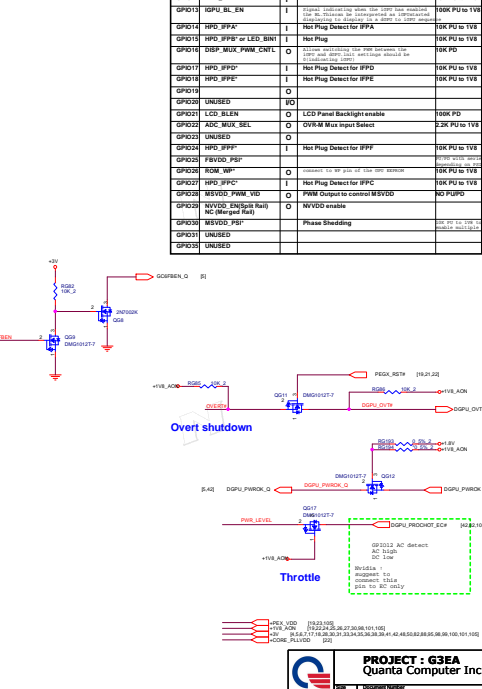
Size A	Document Number PCH(NA)	Rev 1A
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[illegible][illegible]

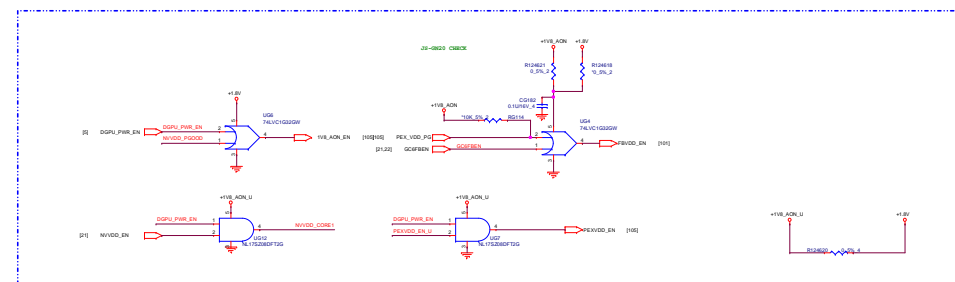
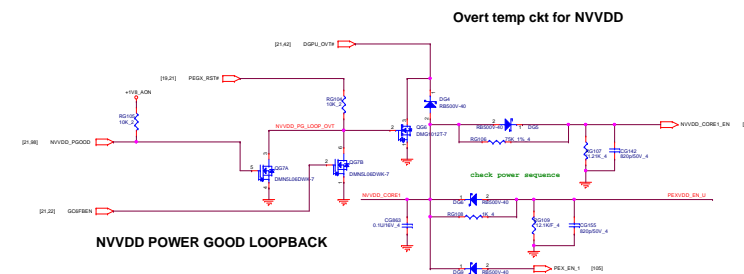
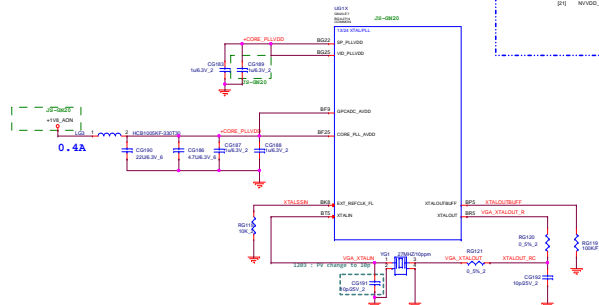
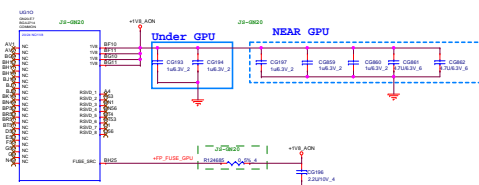
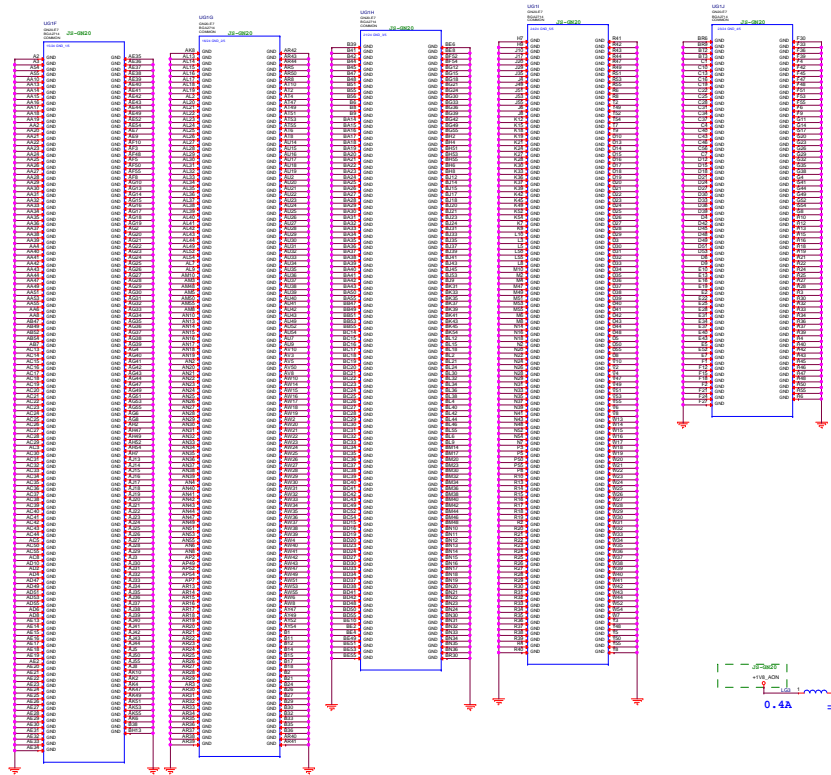
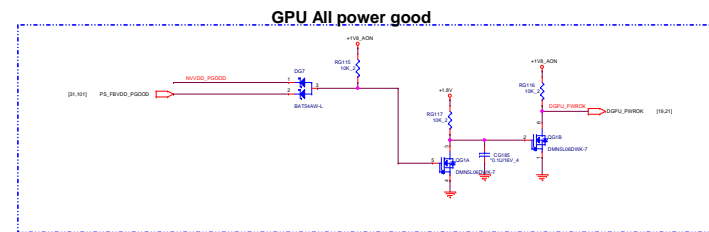


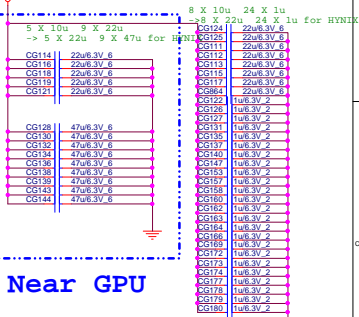
Table 4.6 Low Power State Summary

Low Power Features	TV	NV2	MSVD	NVDD	PCDD	VPP	PCDD	V3	FWP
Normal Operation	ON	ON	ON	ON	ON	ON	ON	ON	ON
P-State & Rail Gating (NVDD & MSVD split)	ON	ON	OFF	ON	ON	ON	ON	ON	ON
P-State & Rail Gating (NVDD & MSVD merged)	ON	ON	ON	ON	ON	ON	ON	ON	ON
GO-D	ON	ON	OFF	OFF	ON	ON	ON	ON	ON
OC-D	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON
OE	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF

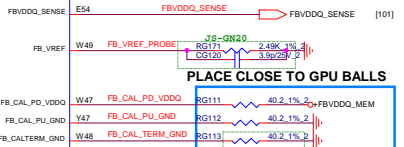


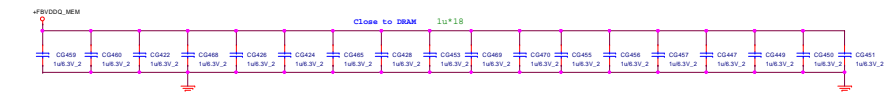
+FBVDDQ_MEM	[19,20,23,24,25,26,27,101]
+V18_AON	[19,21,24,25,26,27,30,98,101,102]
+2V	[4,5,6,7,7,7,18,21,28,30,31,32,34,35,36,38,39,41,42,48,50,82,88,95,98,99,100,101,102]
+1.8V	[4,7,21,39,41,88,95]

Under GPU

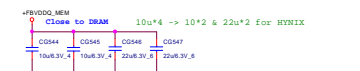
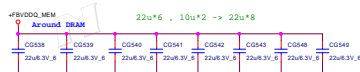
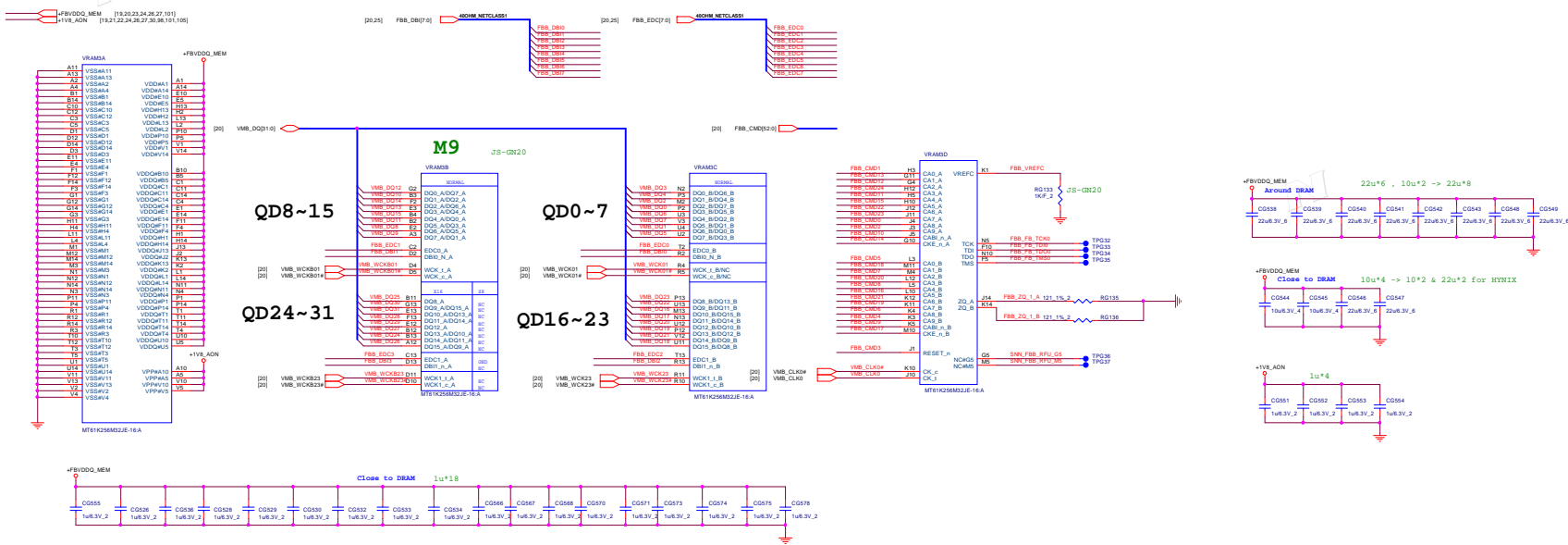


Near GPU

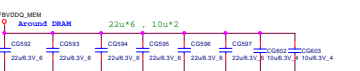
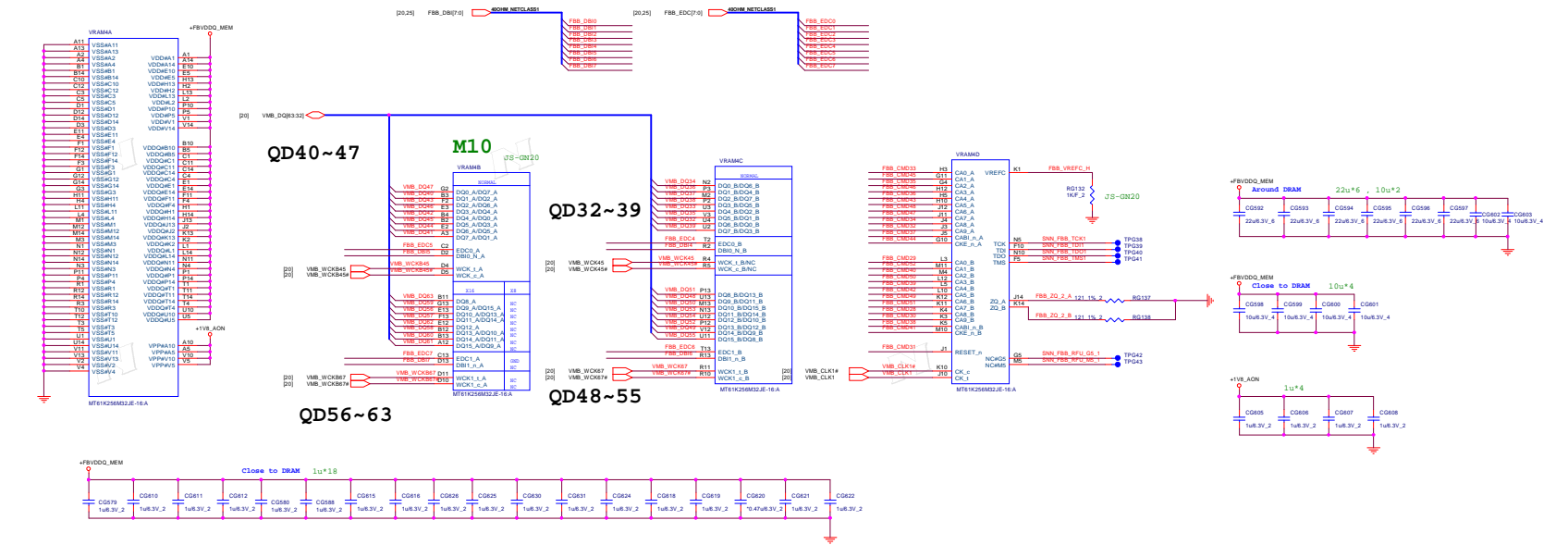


[illegible]

GDDR6 CMD Mapping		x16 Mode	
Lower 0..31		Upper 32..63	
DRAM1		DRAM2	
CHA-Byte 0,1		CHA-Byte 4,5	
CA0_A	CMD0	CMD20	
CA1_A	CMD9	CMD28	
CA2_A	CMD8	CMD21	
CA3_A	CMD32	CMD29	
CA4_A	CMD7	CMD23	
CA5_A	CMD11	CMD27	
CA6_A	CMD15	CMD30	
CA7_A	CMD14	CMD31	
CA8_A	CMD3	CMD19	
CA9_A	CMD1	CMD17	
CABT_A	CMD6	CMD22	
CKE_A	CMD10	CMD26	
	CHB-Byte 2,3	CHB-Byte 6,7	
CA0_B	CMD4	CMD16	
CA1_B	CMD12	CMD25	
CA2_B	CMD5	CMD24	
CA3_B	CMD13	CMD33	
CA4_B	CMD7	CMD23	
CA5_B	CMD11	CMD27	
CA6_B	CMD15	CMD30	
CA7_B	CMD14	CMD31	
CA8_B	CMD3	CMD19	
CA9_B	CMD1	CMD17	
CABT_B	CMD6	CMD22	
CKE_B	CMD10	CMD26	
RESET*	CMD2	CMD18	

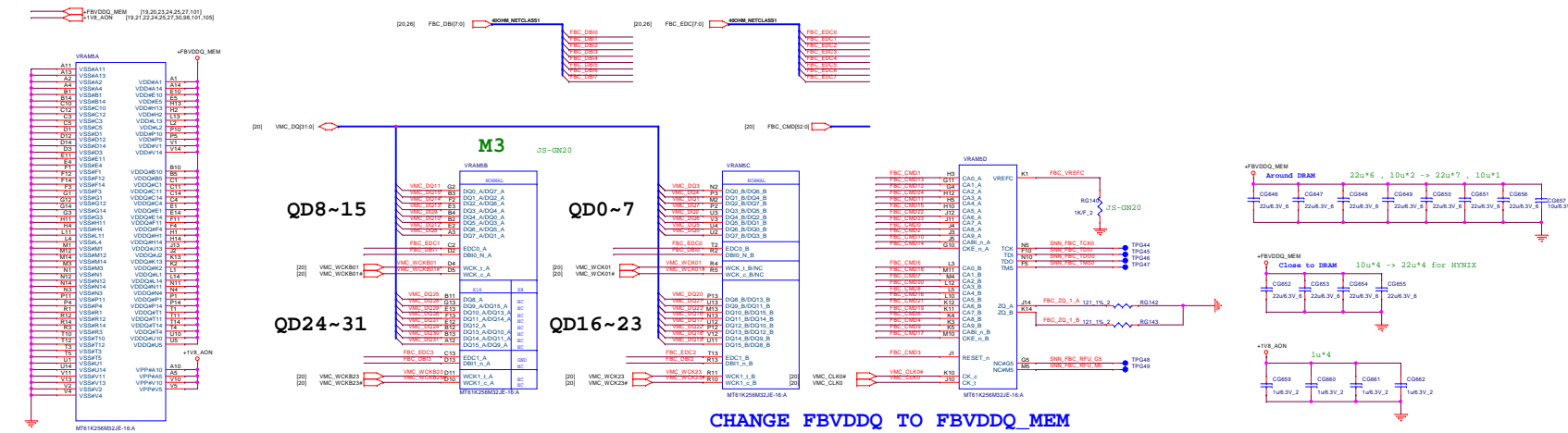


MEMORY: FBB Partition 63..32

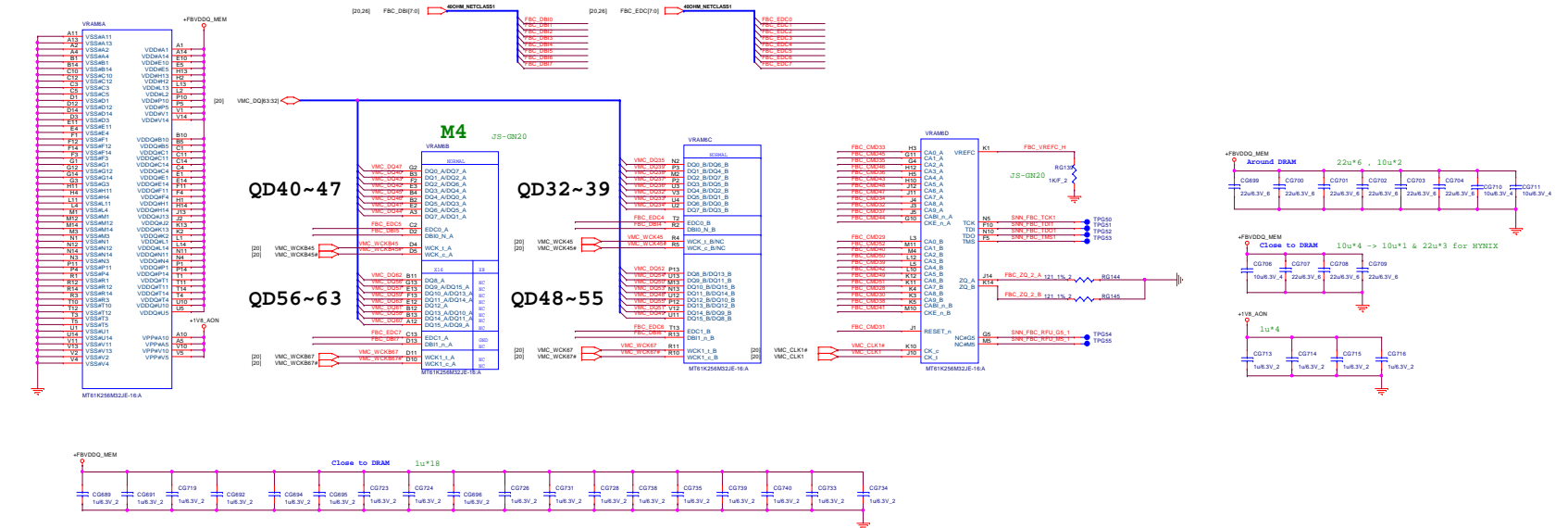


GDDR6 CMD Mapping		x16 Mode
Lower 0..31		Upper 32..63
DRAM1		DRAM2
CHA-Byte 0,1		CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABT_A	CMD6	CMD22
CKE_A	CMD10	CMD26
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABT_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

MEMORY: FBC Partition 31..0



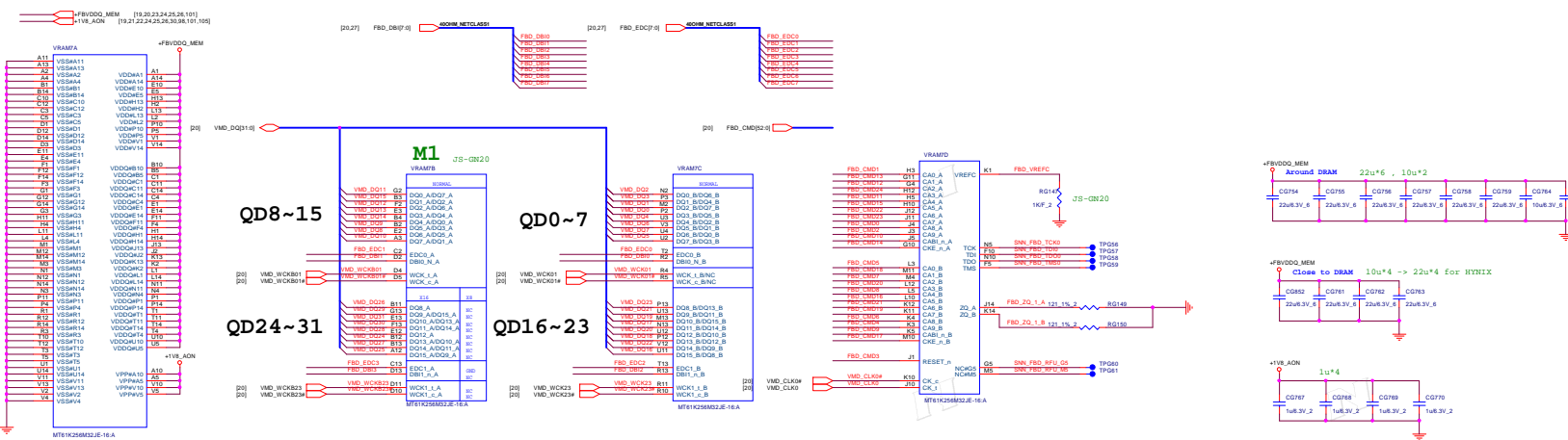
MEMORY: FBC Partition 63..32



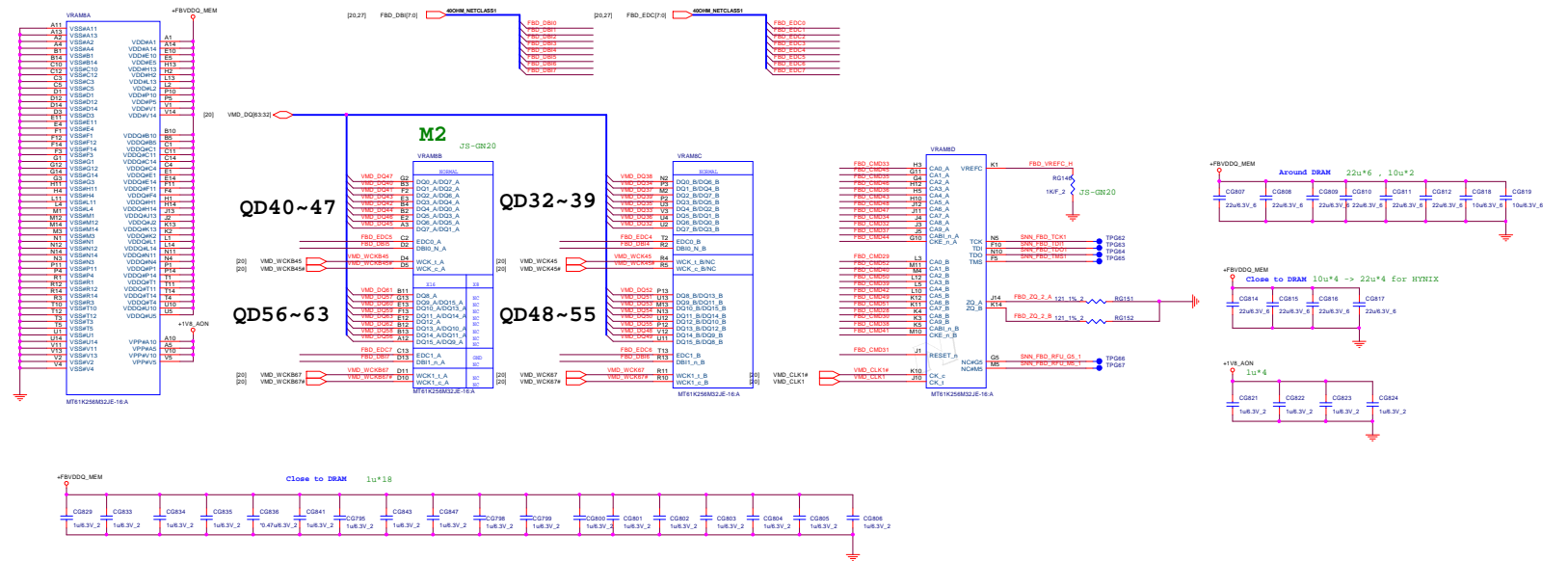
GDDR6 CMD Mapping		x16 Mode
Lower 0..31	DRAM1	Upper 32..63
CH-Byte 0,1	DRAM2	CH-Byte 4,5

CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD8	CMD21
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD15	CMD30
CA6_A	CMD14	CMD31
CA7_A	CMD3	CMD19
CA8_A	CMD1	CMD17
CAB1_A	CMD6	CMD22
CKE_A	CMD10	CMD26
CHB-Byte 2,3		CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CAB1_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

MEMORY: FBD Partition 31..0

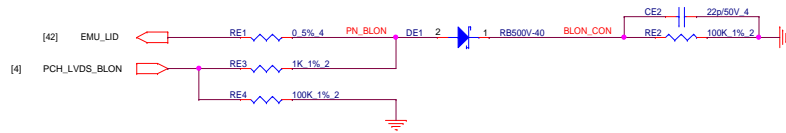


MEMORY: FBD Partition 63..32



GDDR6 CMD Mapping		x16 Mode
Lower 0..31		Upper 32..63
DRAM1		DRAM2
CHA-Byte 0,1		CHA-Byte 4,5
CA0_A	CMD0	CMD20
CA1_A	CMD9	CMD28
CA2_A	CMD1	CMD31
CA3_A	CMD32	CMD29
CA4_A	CMD7	CMD23
CA5_A	CMD11	CMD27
CA6_A	CMD15	CMD30
CA7_A	CMD14	CMD31
CA8_A	CMD3	CMD19
CA9_A	CMD1	CMD17
CABT_A	CMD6	CMD22
CKE_A	CMD10	CMD26
CHB-Byte 2,3		CHB-Byte 6,7
CA0_B	CMD4	CMD16
CA1_B	CMD12	CMD25
CA2_B	CMD5	CMD24
CA3_B	CMD13	CMD33
CA4_B	CMD7	CMD23
CA5_B	CMD11	CMD27
CA6_B	CMD15	CMD30
CA7_B	CMD14	CMD31
CA8_B	CMD3	CMD19
CA9_B	CMD1	CMD17
CABT_B	CMD6	CMD22
CKE_B	CMD10	CMD26
RESET*	CMD2	CMD18

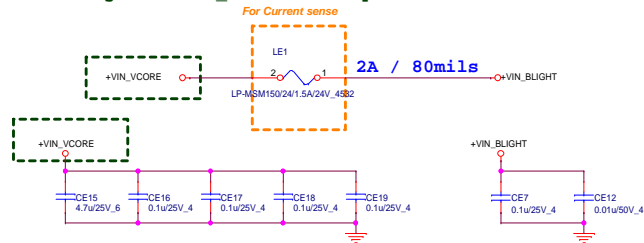
LID Switch



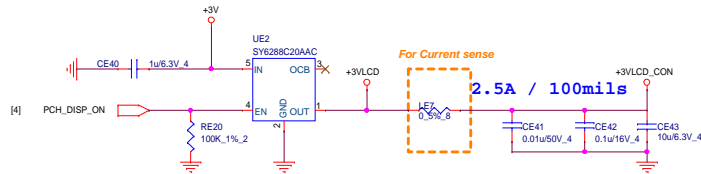
eDP CONN.

LCD Backlight

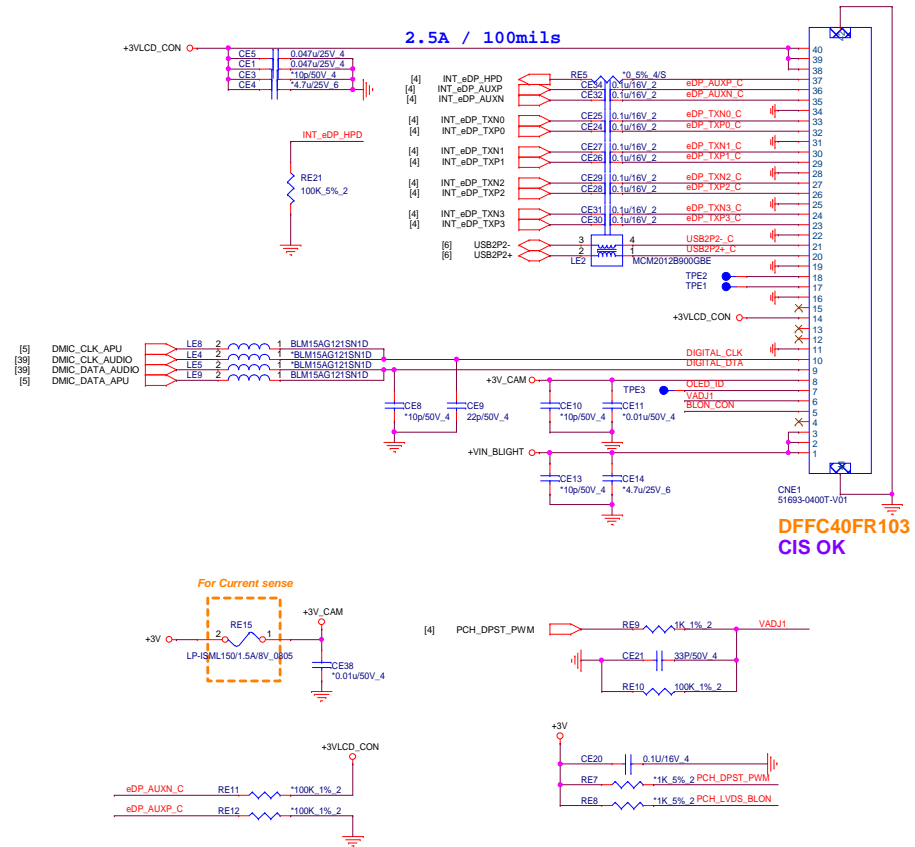
+VIN change to +VIN_VCORE for layout!




3V LCD Power SW



IR CAM Power SW

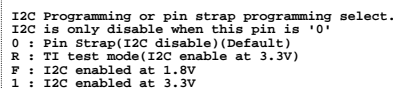


NA

	PROJECT : G3EF Quanta Computer Inc.		
	Size A	Document Number eDP Mux PS8461(NA)	Rev 1A
	Date: Thursday, October 08, 2020 Sheet 29 of 106		



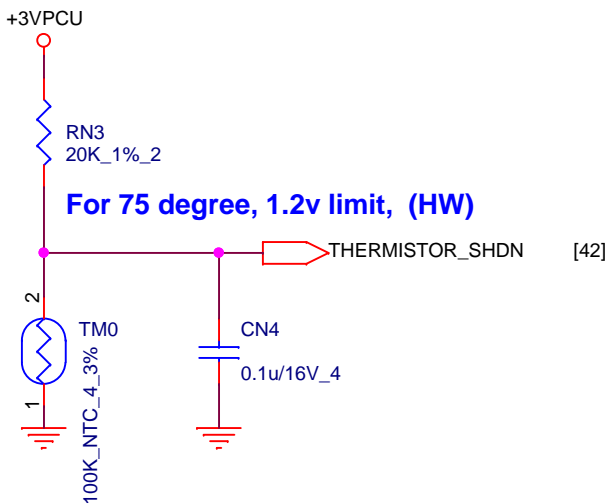
Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DF_PWR



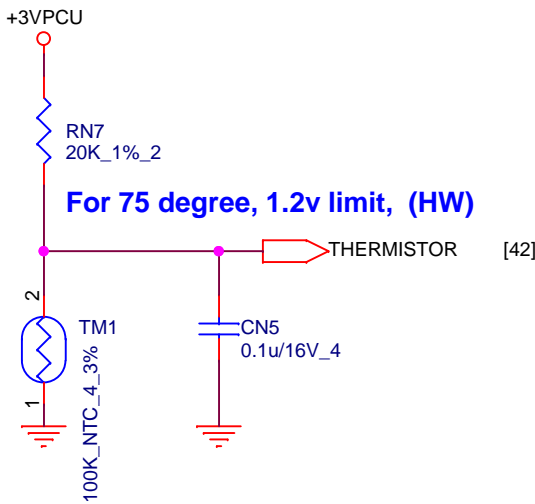
DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C EN is not '0' DPEQ0 sets I2C address



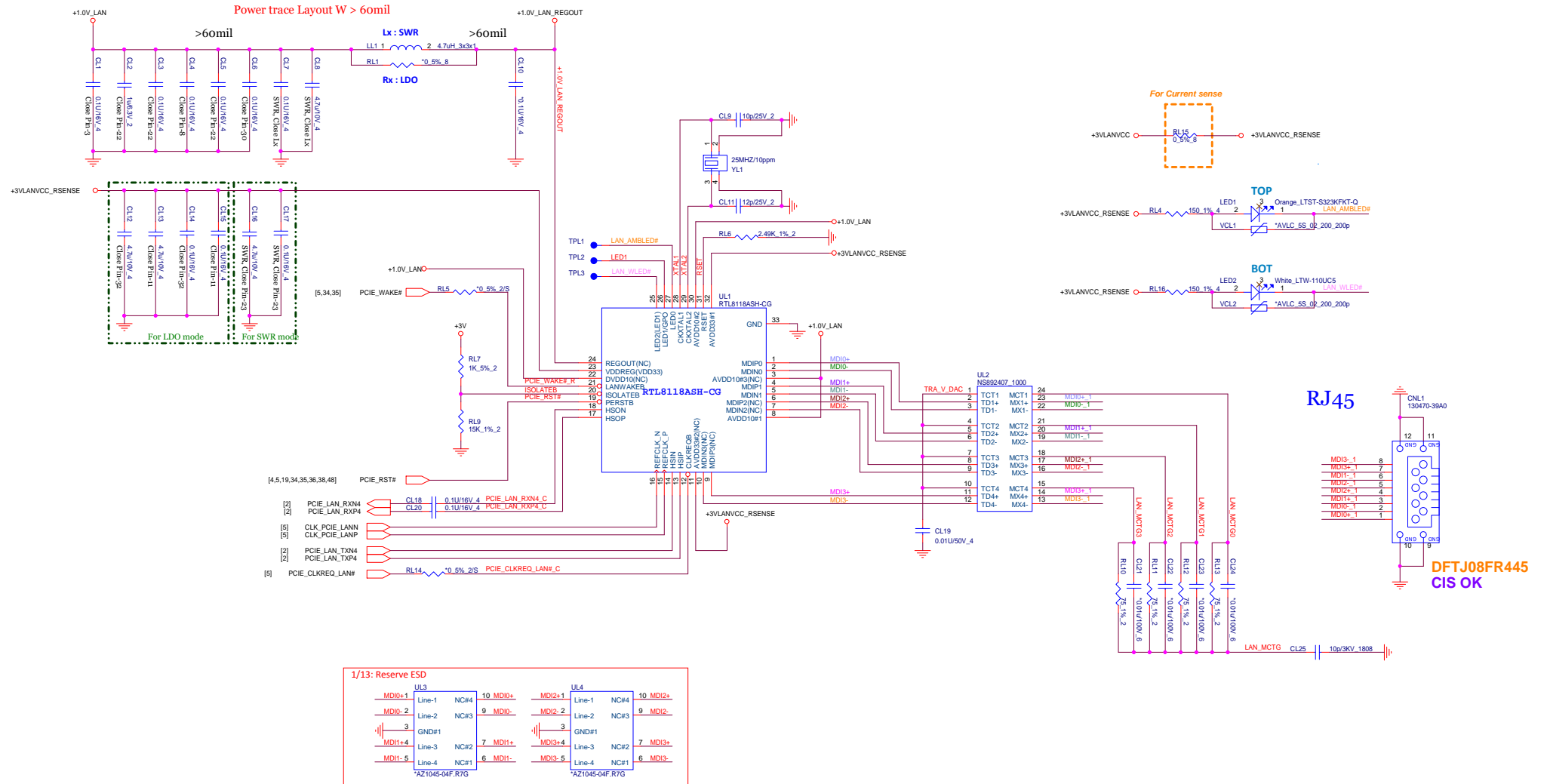
For HW shutdown (TOP nearby CPU)



For CPU (Bottom nearby CPU)



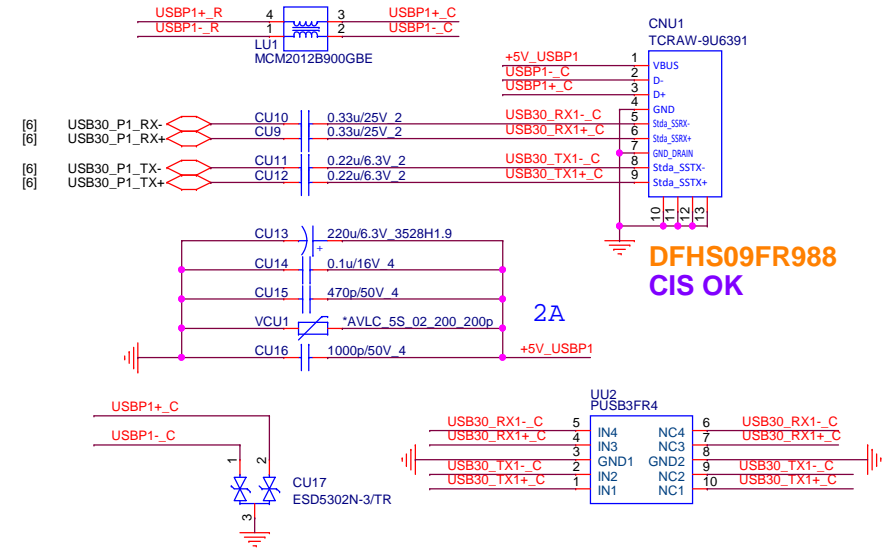
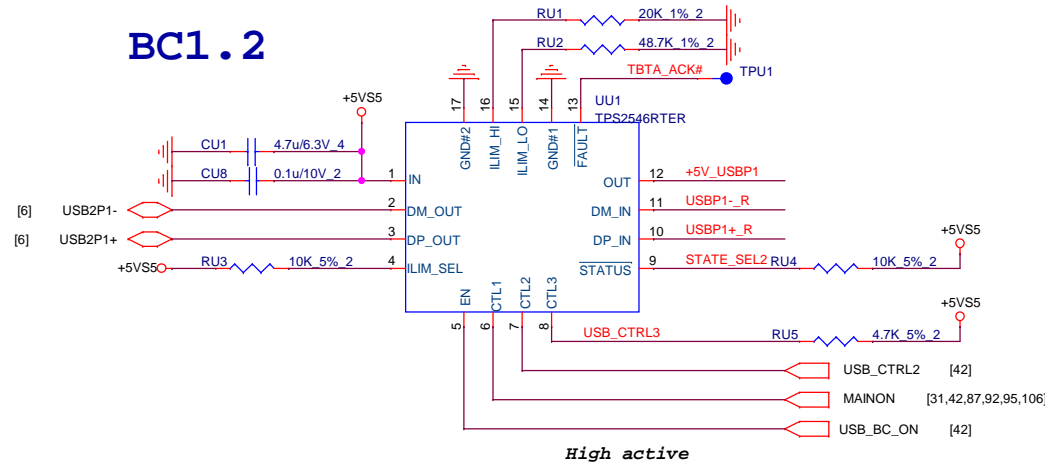
LAN & RJ45



USB 2.0/3.0 Combo MB

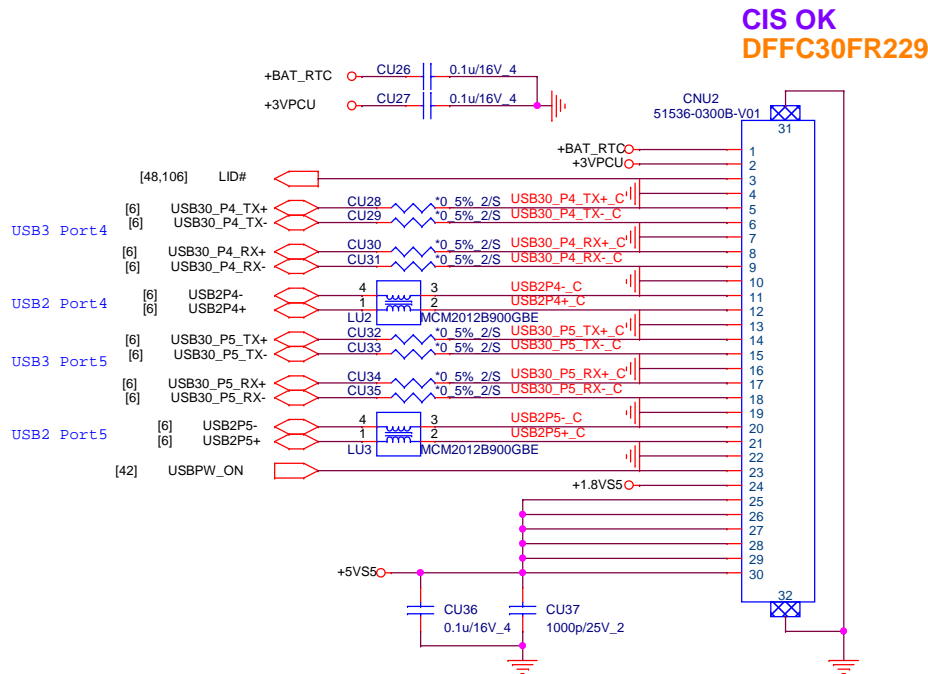
34

BC1.2

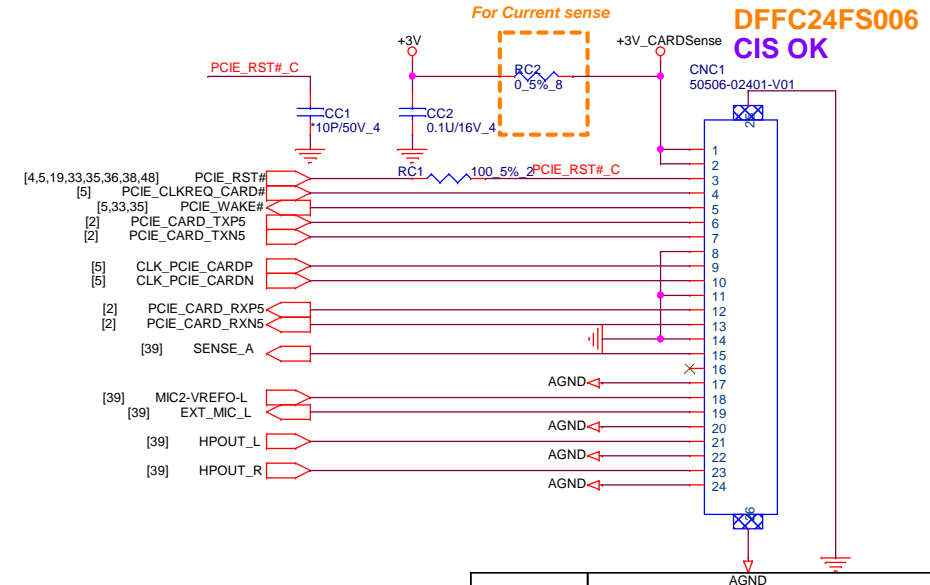


DFHS09FR988
CIS OK

USB small board



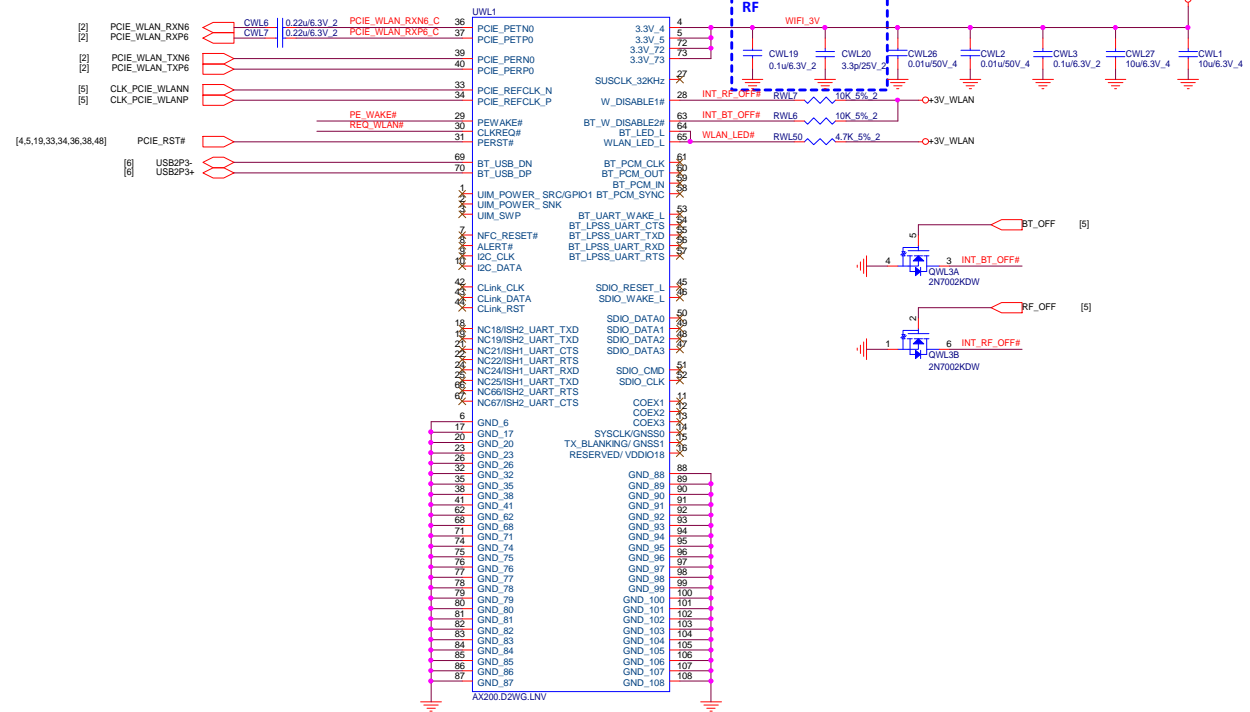
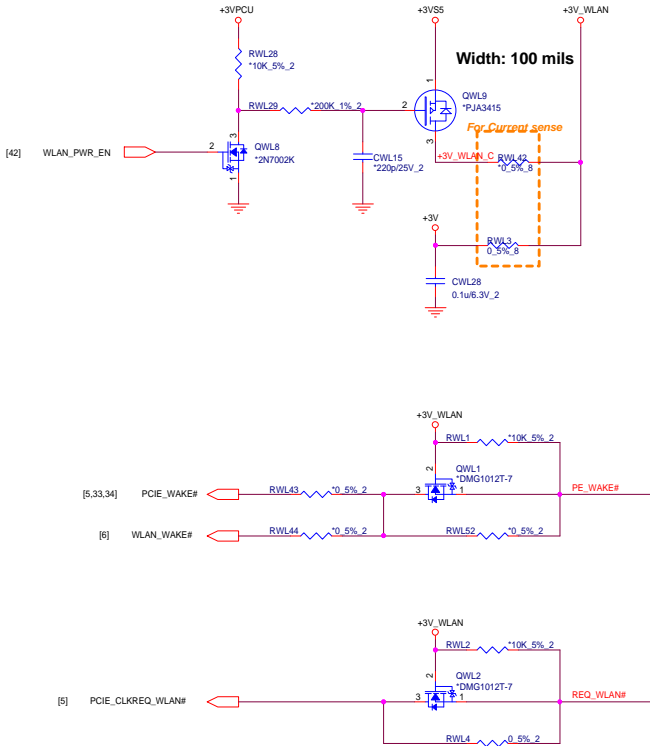
SD Card Audio Jack to Small Board



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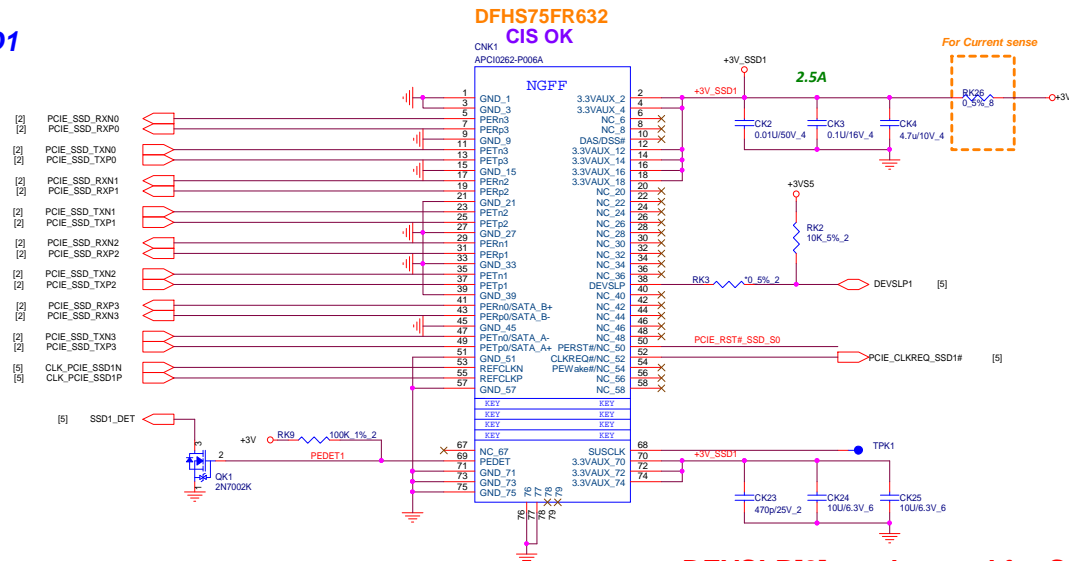
Size	Document Number	Rev
B	USB3.0/SD/USB Small Board	3A
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Reserve WLAN wake function for NV GPU

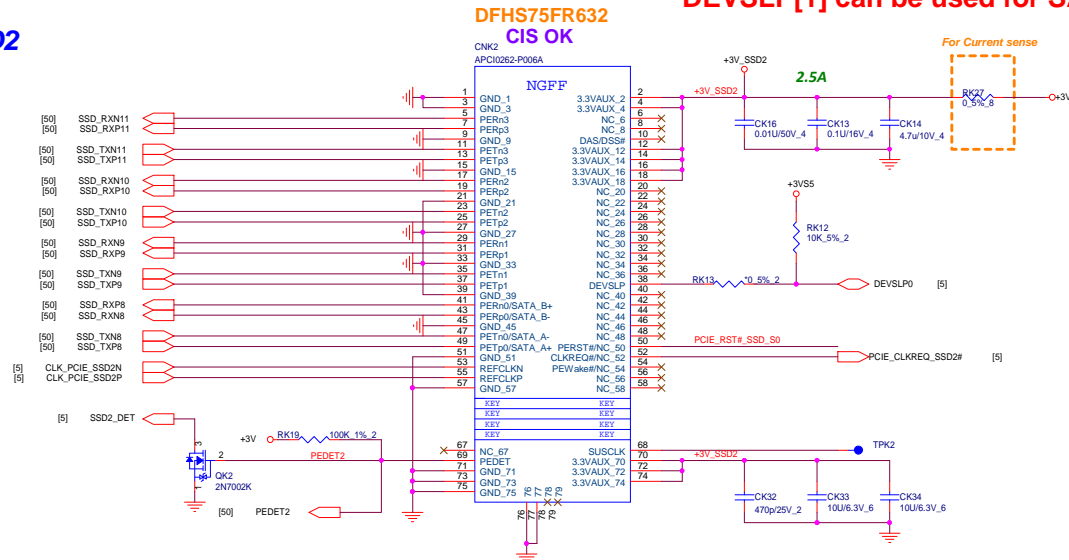


Cyclone Peak 2	ADPCAX2013	WL/BT 802.11ABGNACAX AX200.D2WG.LNV
	ADPCAX2024	WL/BT 802.11ABGNACAX AX200.D2WG.LNVTOPBS

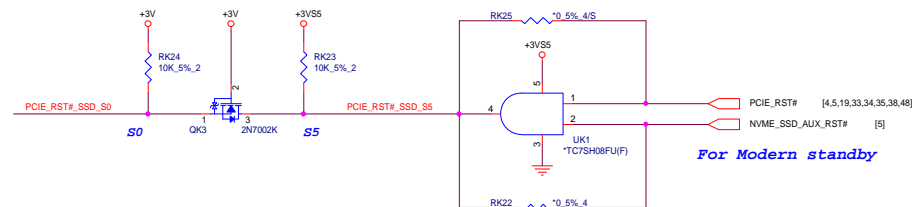
SSD1



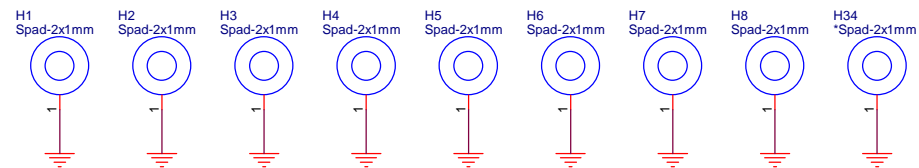
SSD2



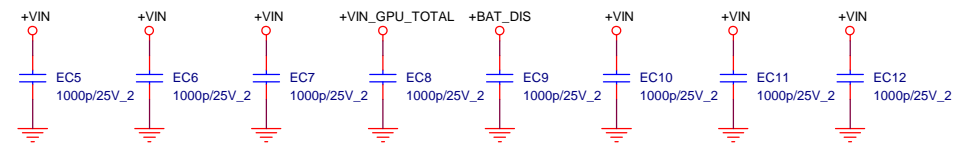
For leakage



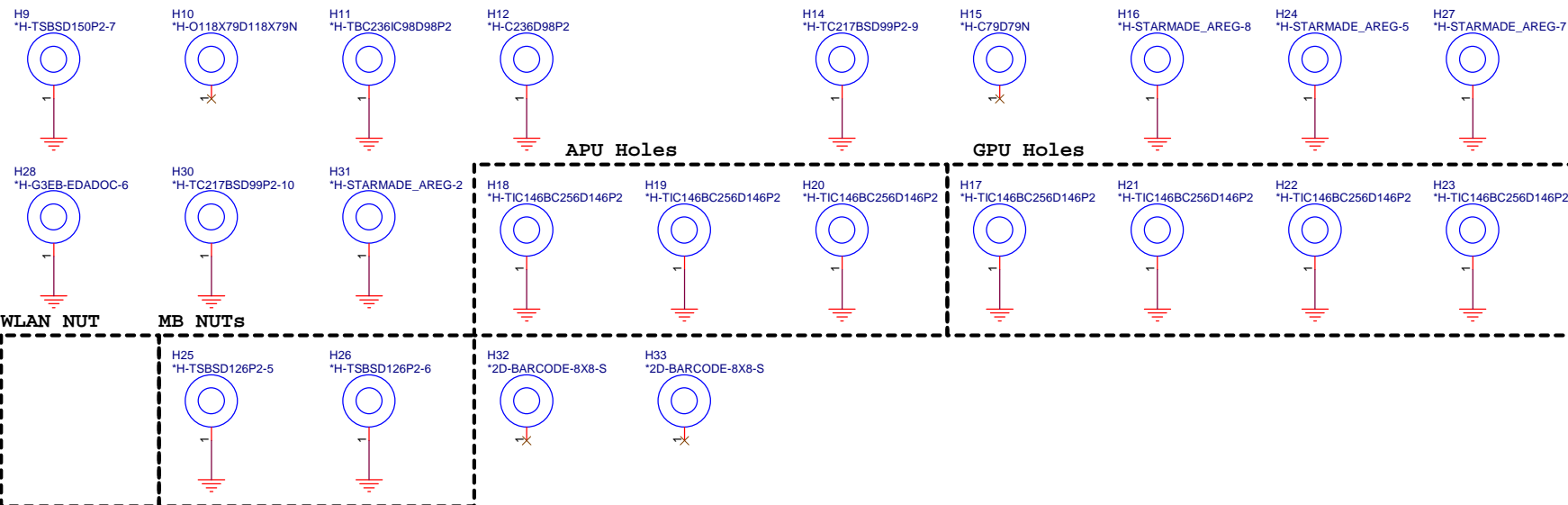
EMI PAD



EMI CAP



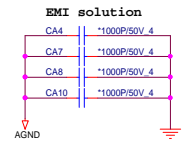
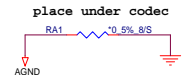
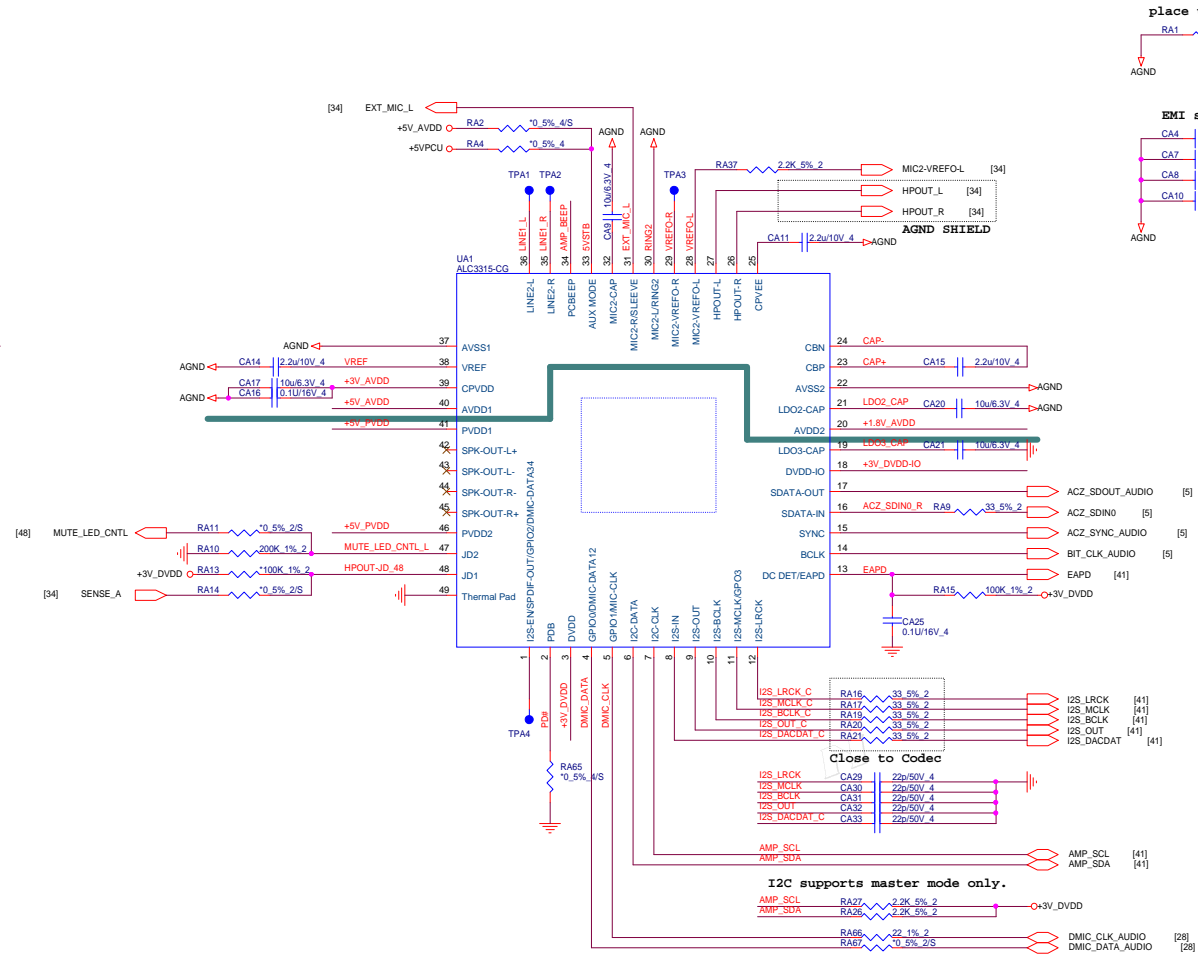
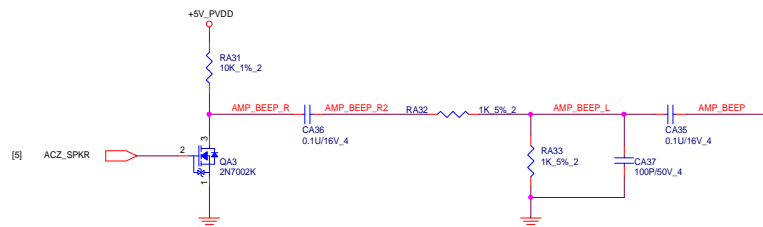
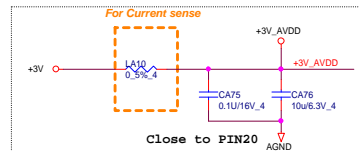
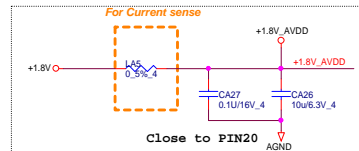
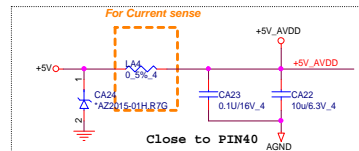
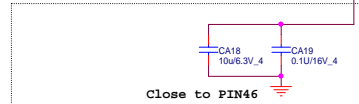
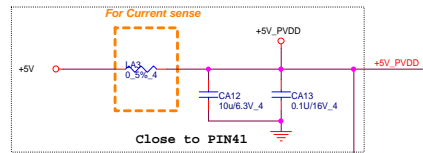
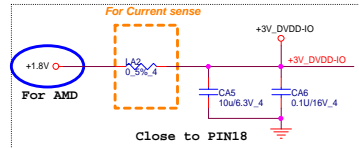
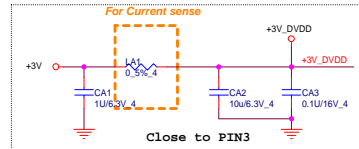
Holes




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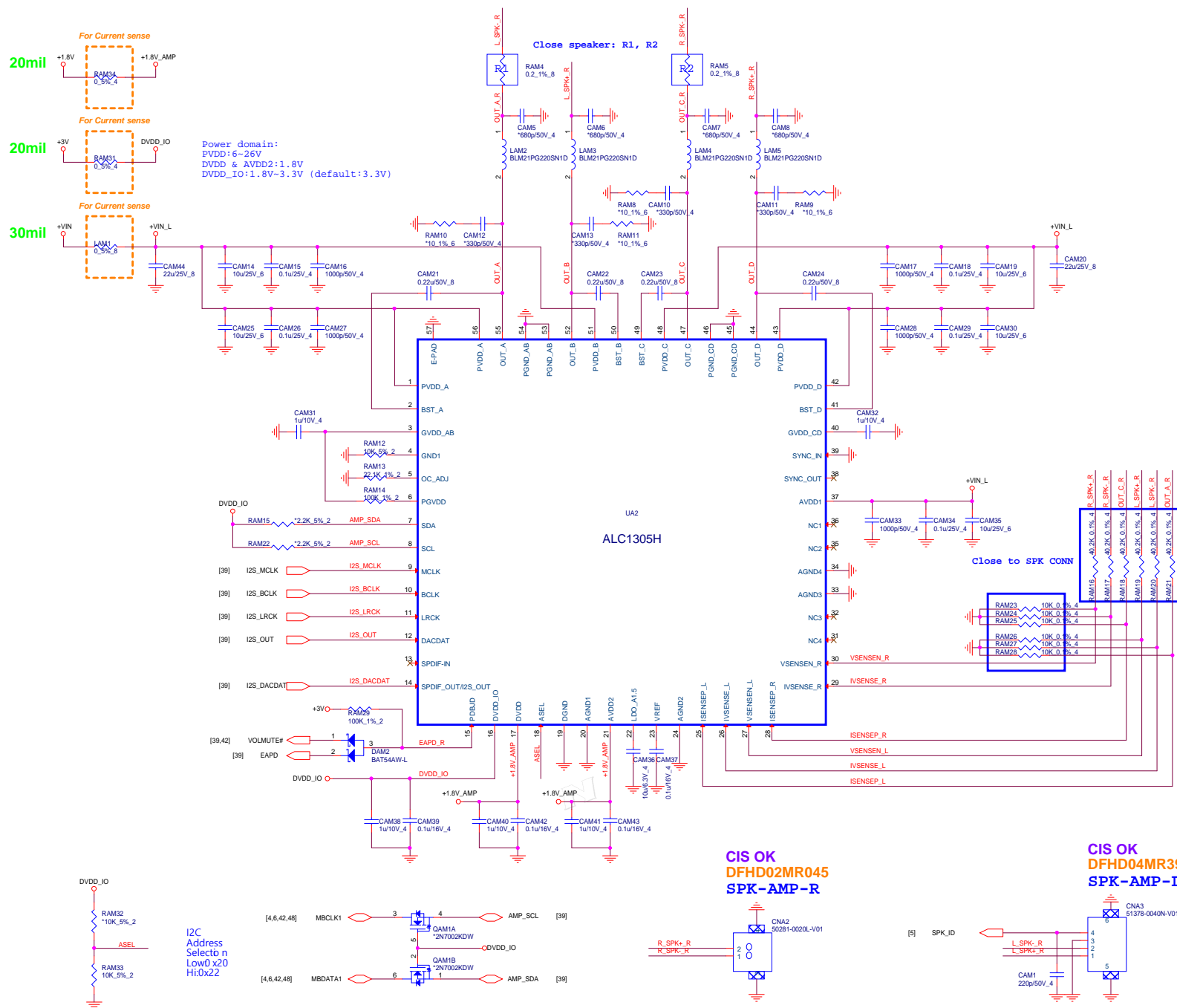
Size B	Document Number EMI/RF Solution/HOLE	Rev 1A
Date: Thursday, October 08, 2020 Sheet 37 of 106		

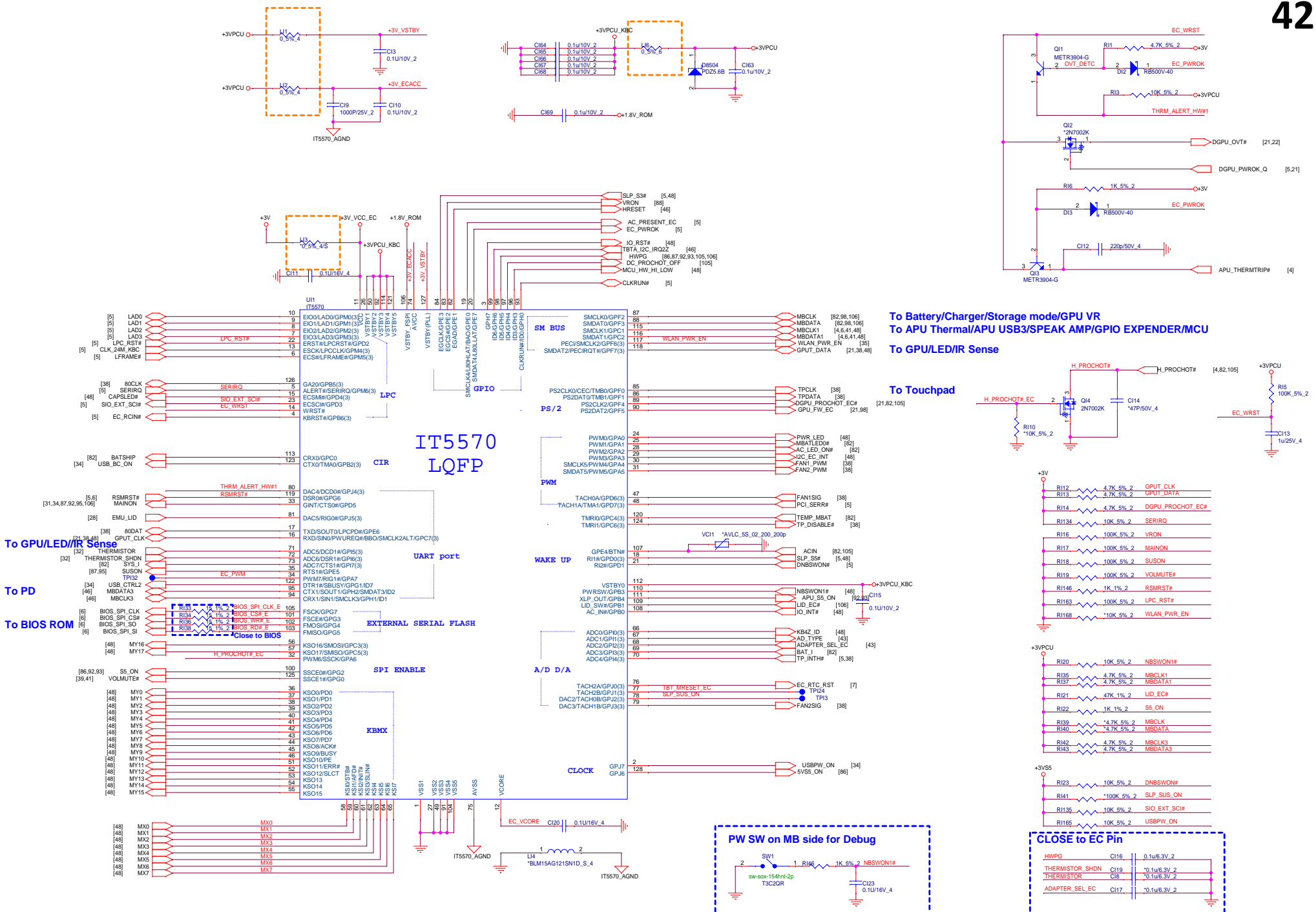
AUDIO CODEC ALC3315-CG



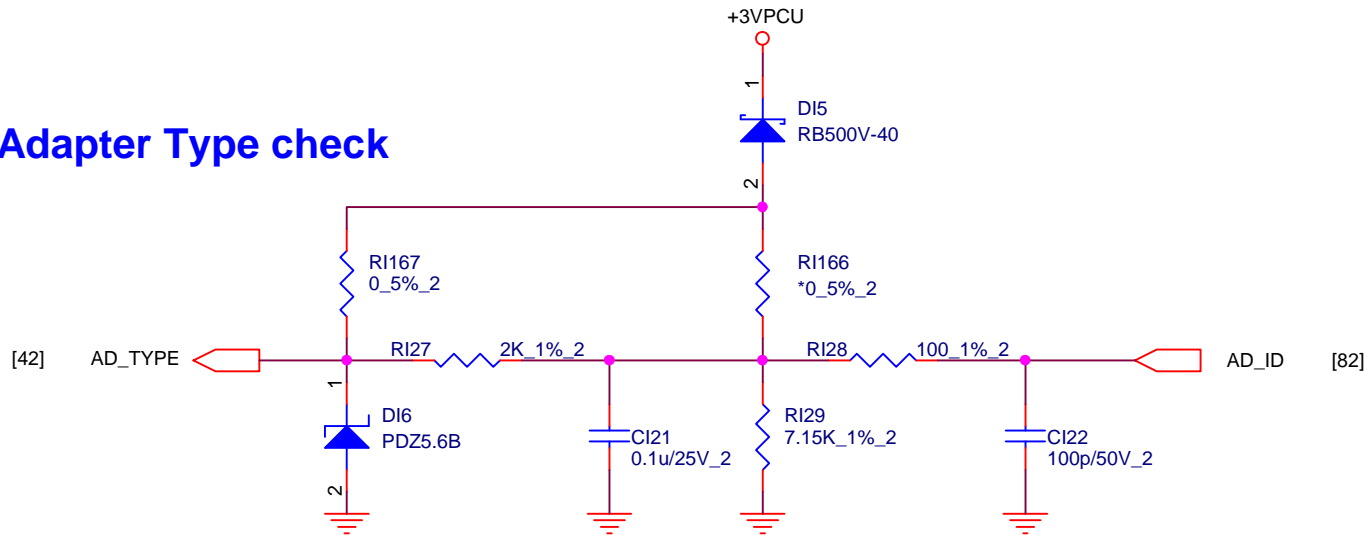
Small Board

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		Size A	Document Number Head Phone Jack(NA)
Date: Thursday, October 08, 2020		Sheet	40 of 106

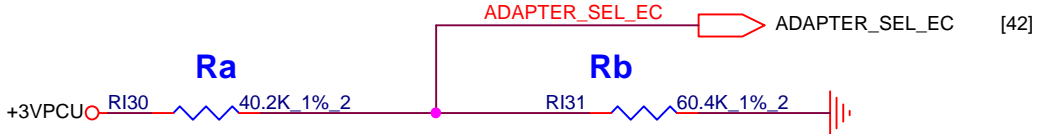





Adapter Type check



Adapter select for EC



	Ra	Rb	ADAPTER_SEL_EC	GPU
200W	40.2K (CS34021FE02)	60.4K (CS36041FE00)	1.981V	GN20-E5 80W Max-Q support up to 100W TGP
200W	90.9K (CS39091FE00)	10K (CS31001FE14)	0.327V	GN20-E3 80W Max-P support up to 100W TGP
200W	49.9K (CS34991FE02)	49.9K (CS34991FE02)	1.650V	GN20-E5 80W Max-Q support up to 80W TGP
200W	69.8K (CS36981FE02)	30.1K (CS33011FE00)	0.994V	GN20-E3 80W Max-P support up to 80W TGP




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Quanta Computer Inc.

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Quanta Computer Inc.

Size A	Document Number TR - TBT (USB2 & DP Part)	Rev 1A
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NA

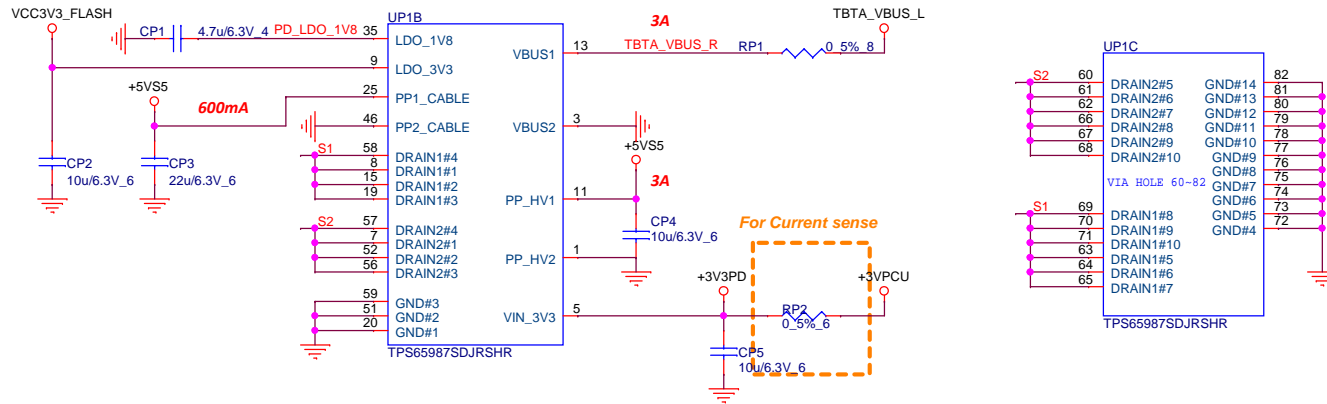


NB5

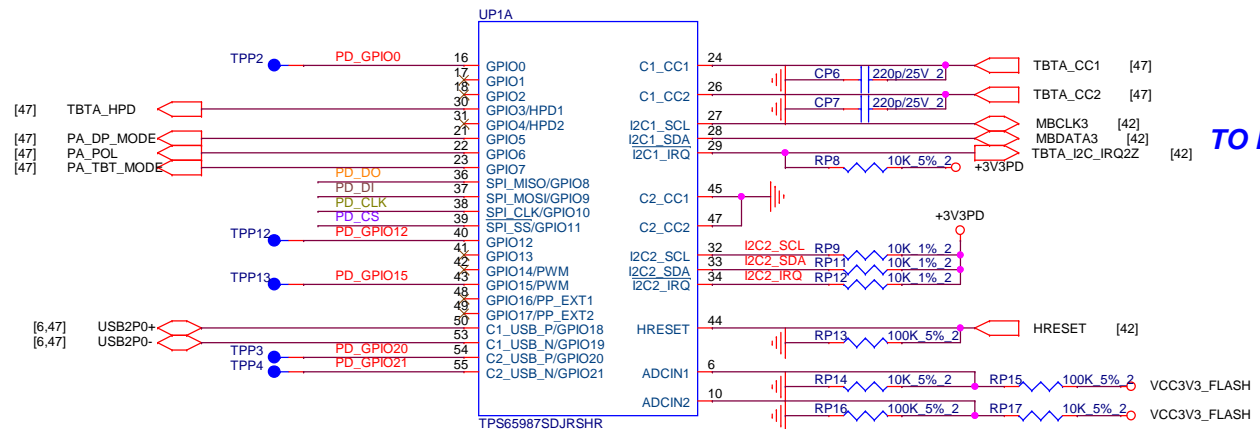
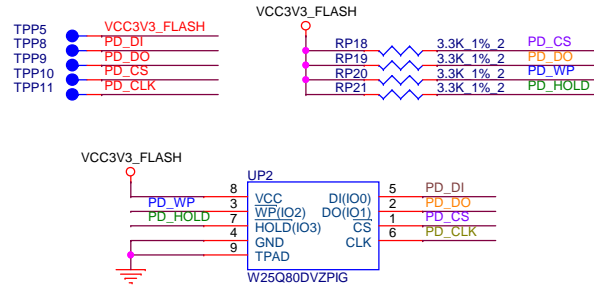
PROJECT : G3EF
Quanta Computer Inc.

Size A	Document Number TR - TBT (USB2 & DP Part)	Rev 1A
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PD TPS65987DDJRSR



PD SPI ROM



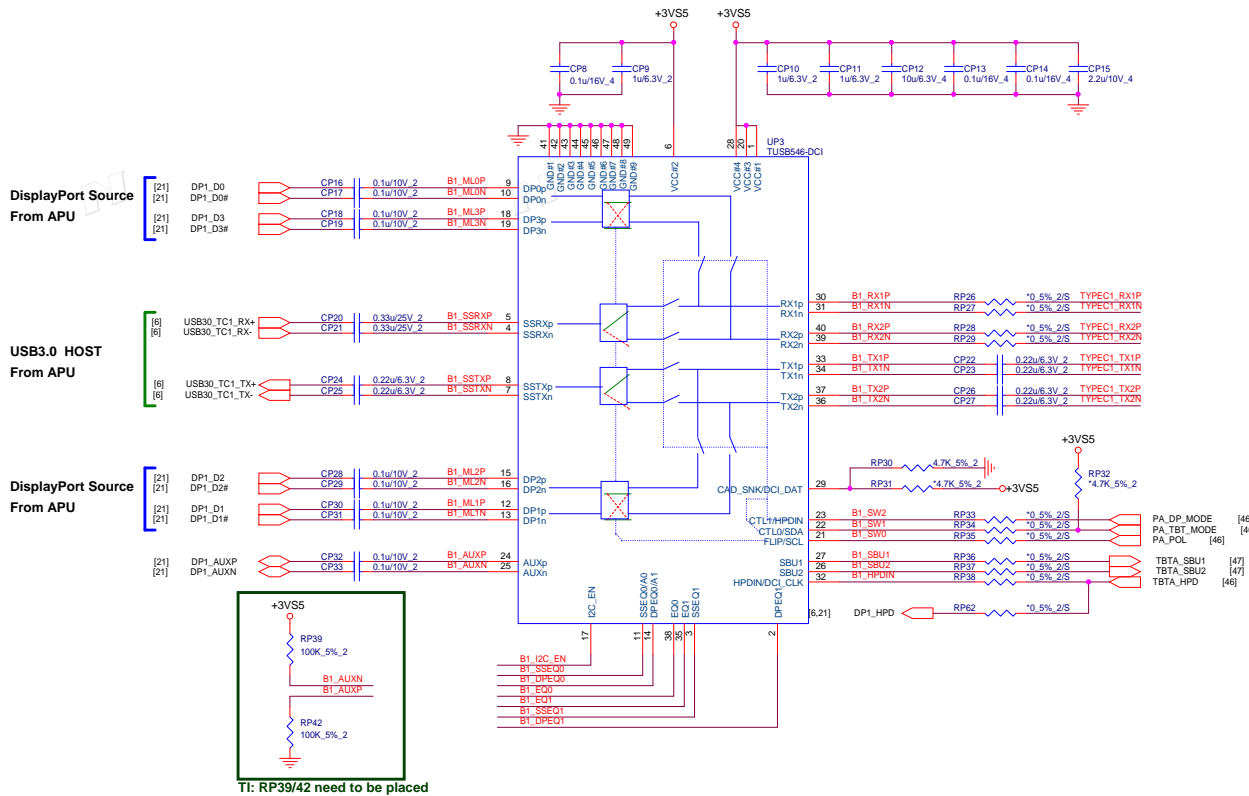
Qunata PN	Part Description
AL180901000	IC OTHER(56P) SN1809018RSR(VQFN)
AL180901003	IC OTHER(56P) SN1809018RSR(VQFN)TOPBS



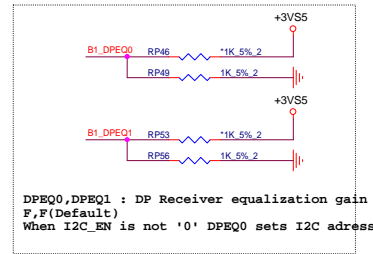
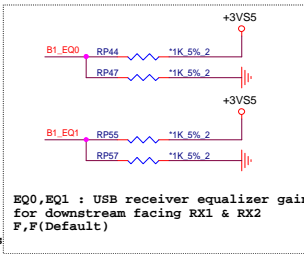
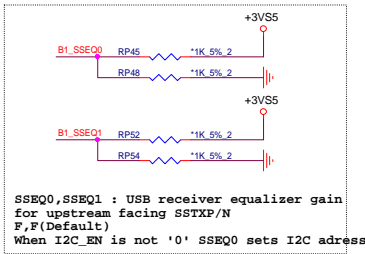
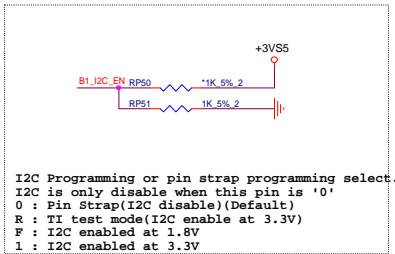
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Size B	Document Number PD TPS65987DDJRSR	Rev 1A
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TI: RP39/42 need to be placed



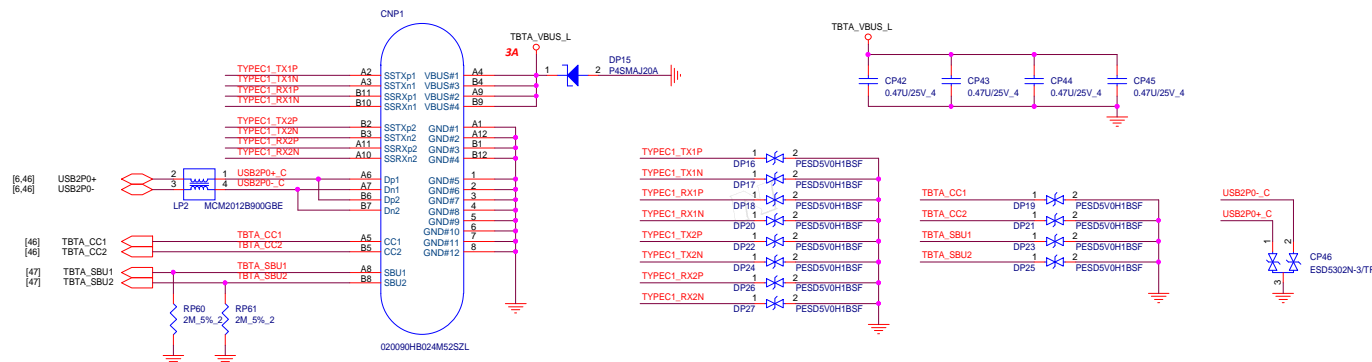
TUSB546 Pin Control Mode

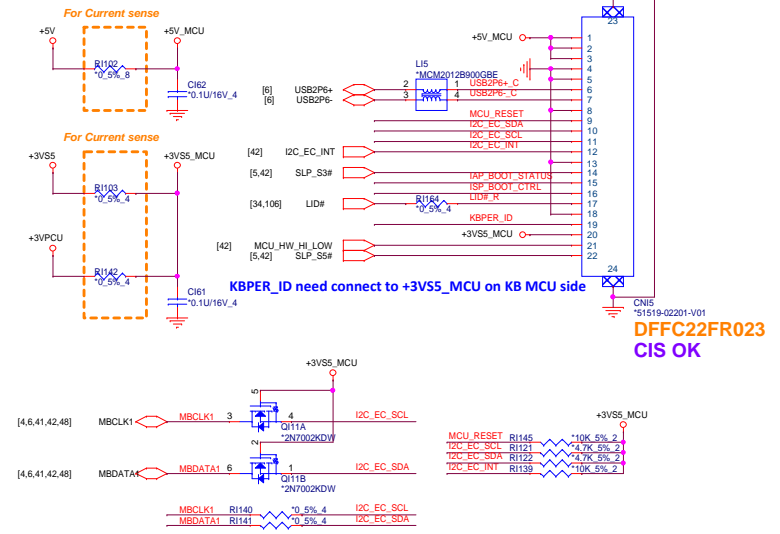
CTL1	FLIP	AUX Select	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

AUX Pin Control Mode

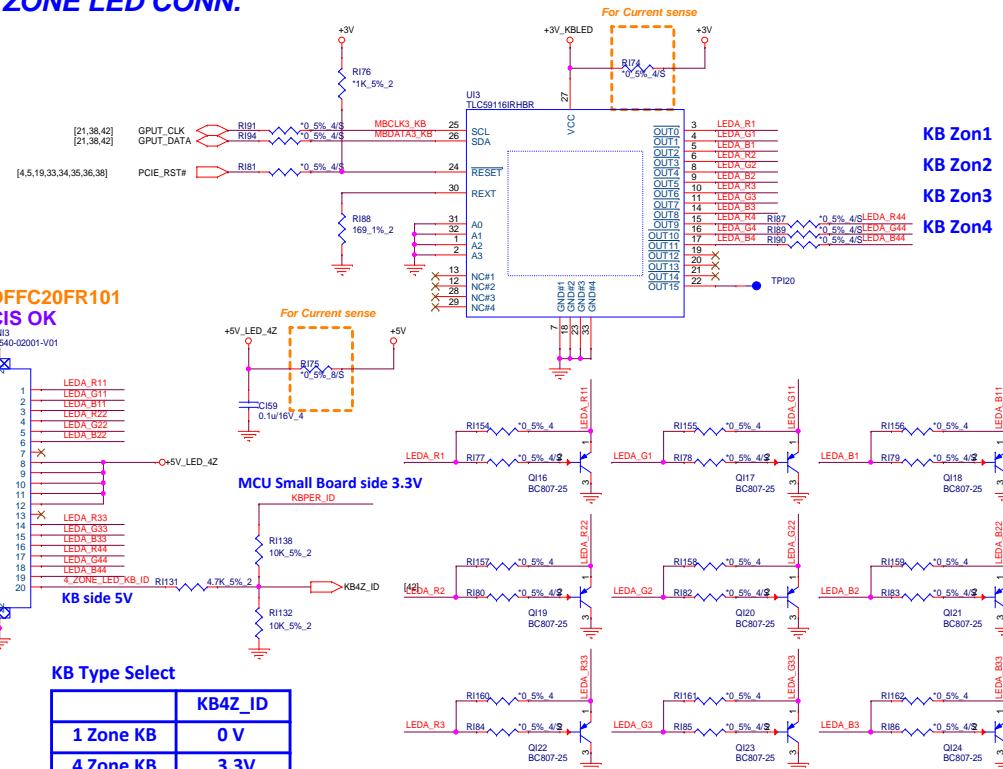
CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L>2ms	X	Open

4 Level Input:
L: Option1 Tie 1Kohm 5% to GND
Option2 Directly tie to GND
R: Tie 20kohm 5% to GND
F: Float(leave pin open)
1: Option1 Tie 1Kohm 5% to Vcc
Option2 Directly tie to Vcc





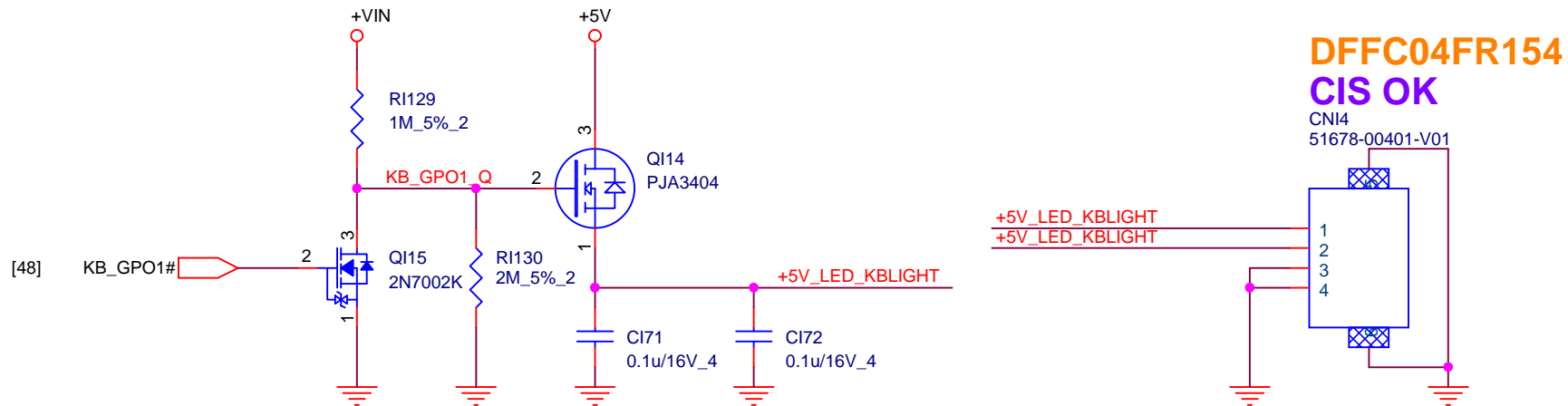
4 ZONE LED CONN.




	KB4Z_ID
1 Zone KB	0 V
4 Zone KB	3.3V
PerKey KB	1.5V


1 zone LED KEYBOARD BACKLIGHT CONN.

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	Size A	Document Number 1 Zone LED	Rev 1A
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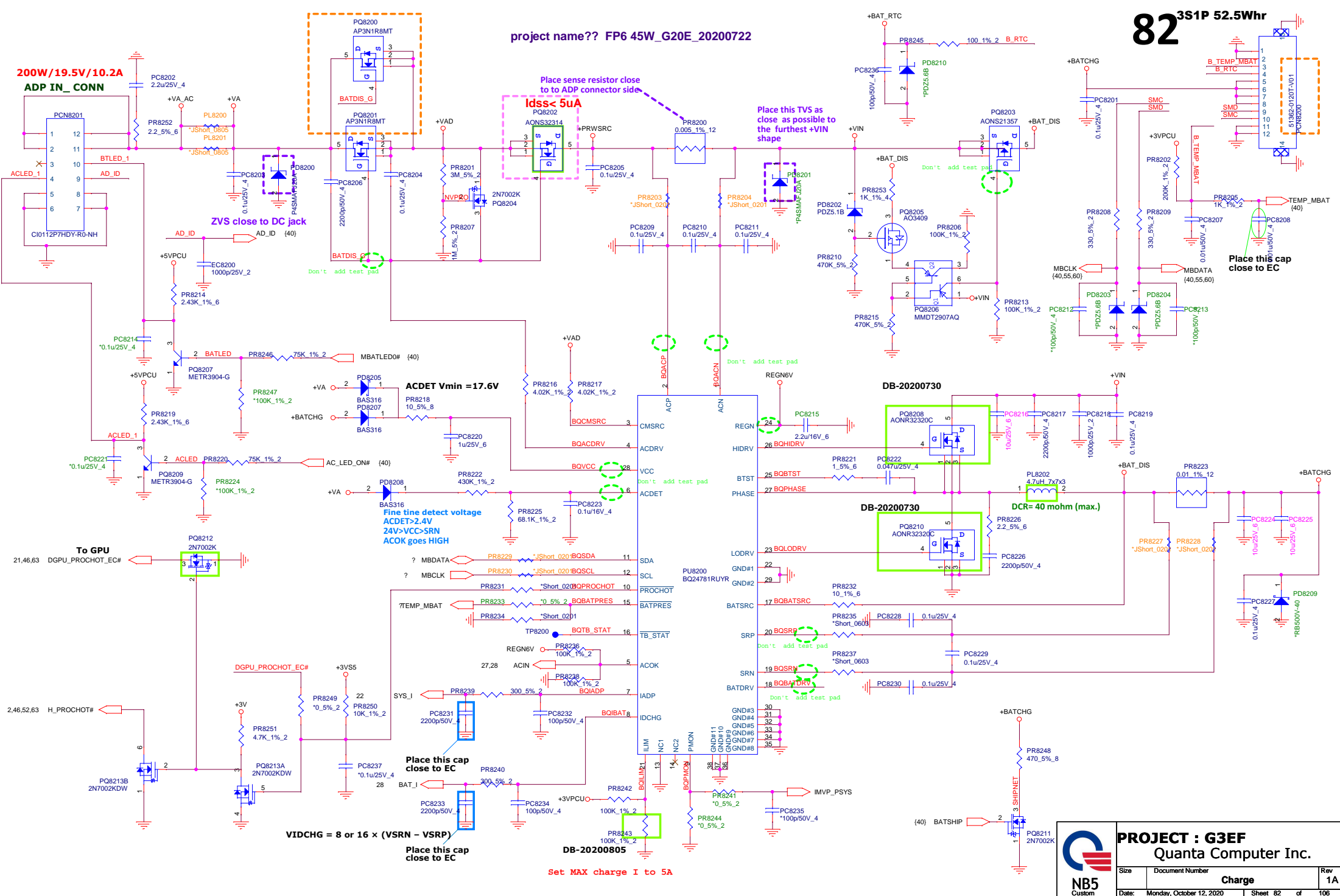
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Quanta Computer Inc.

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NA

NA

project name?? FP6 45W_G20E_20200722

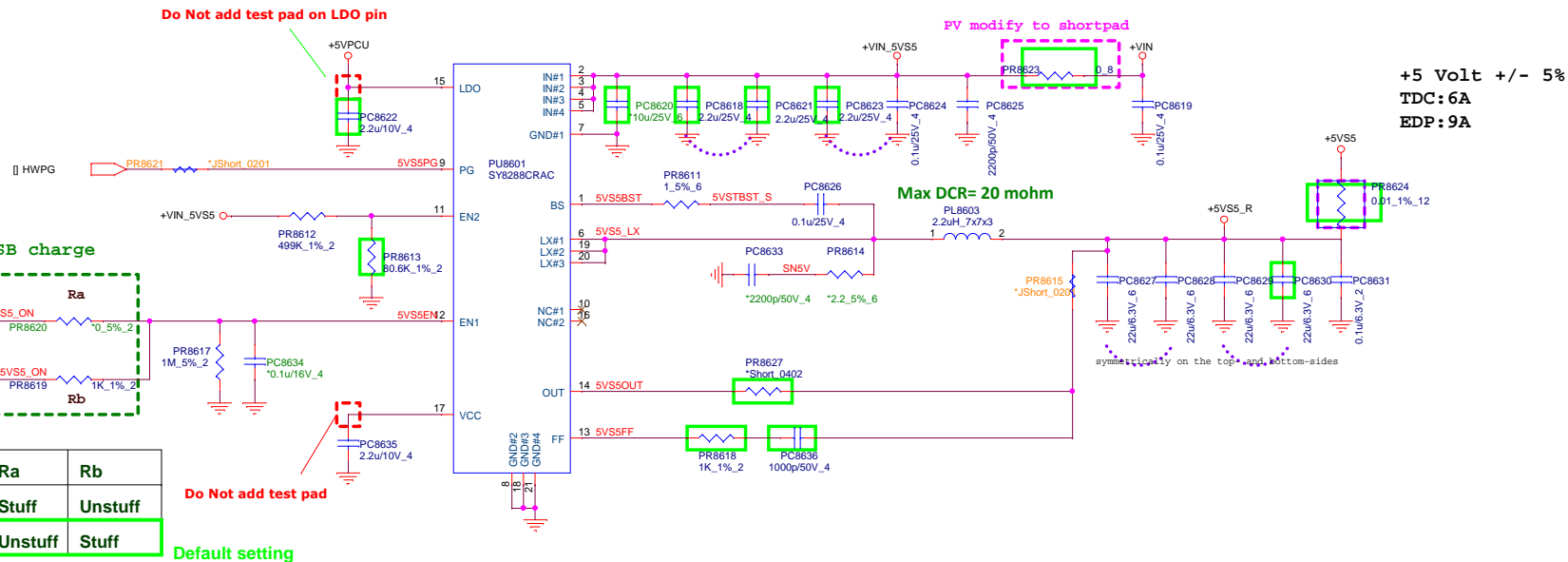
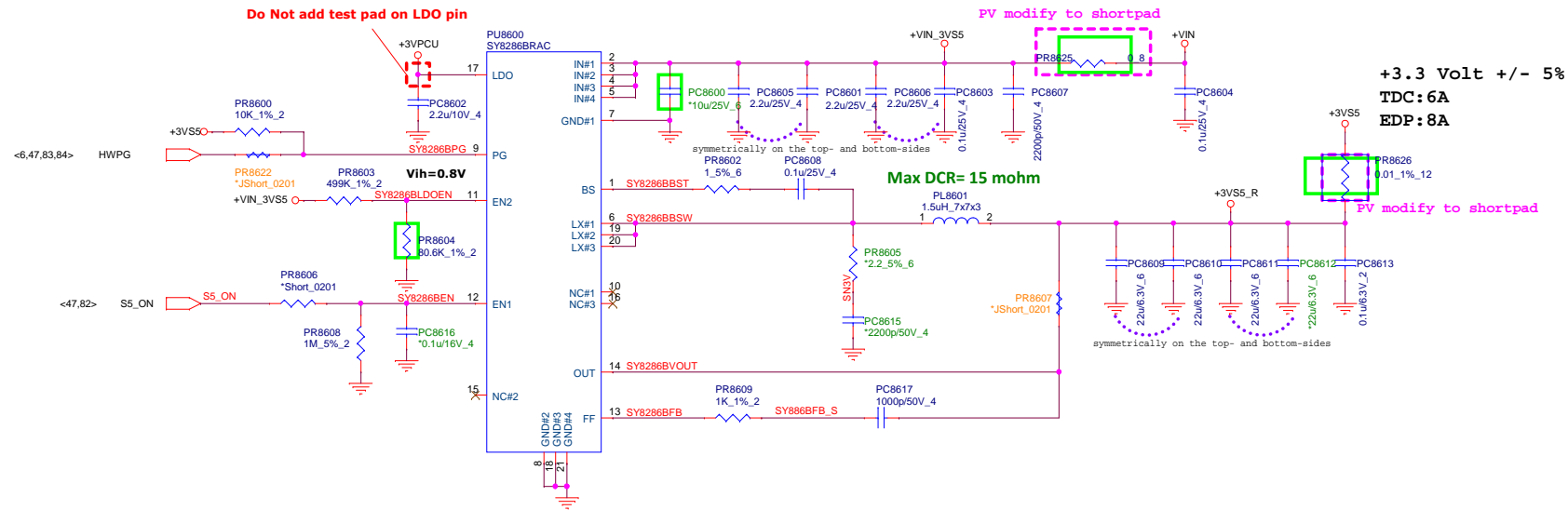


NA

NA

NA

+VIN	<34,50,80,81,83,84,87,88>
+3VS5	<6,12,14,15,17,41,47,63,83,84,85,89>
+5VS5	<6,64,76,83,84,85,86,87,89>
+3VPCU	<15,36,41,47,50,54,81,90>
+5VPCU	<41,81,89>

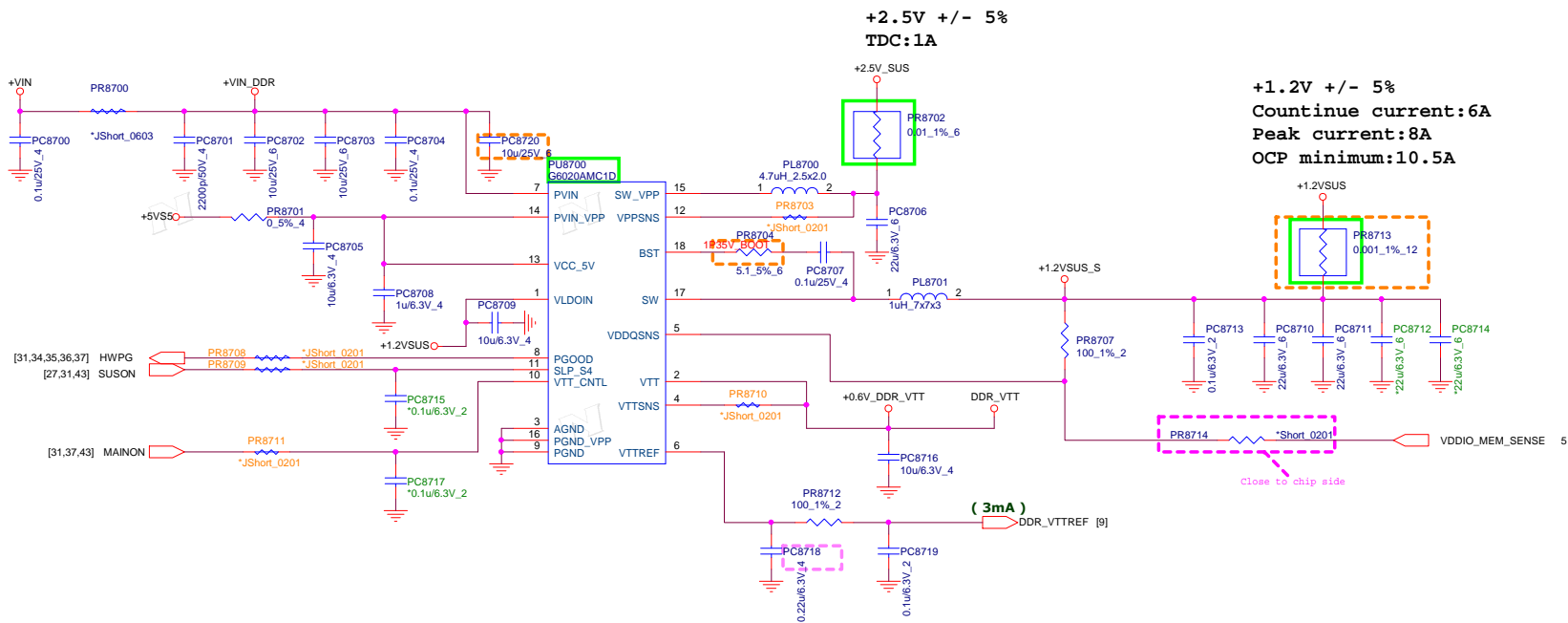


USB Charge support	Ra	Rb
Paviliom(No suport)	Stuff	Unstuff
Envy (Support)	Unstuff	Stuff

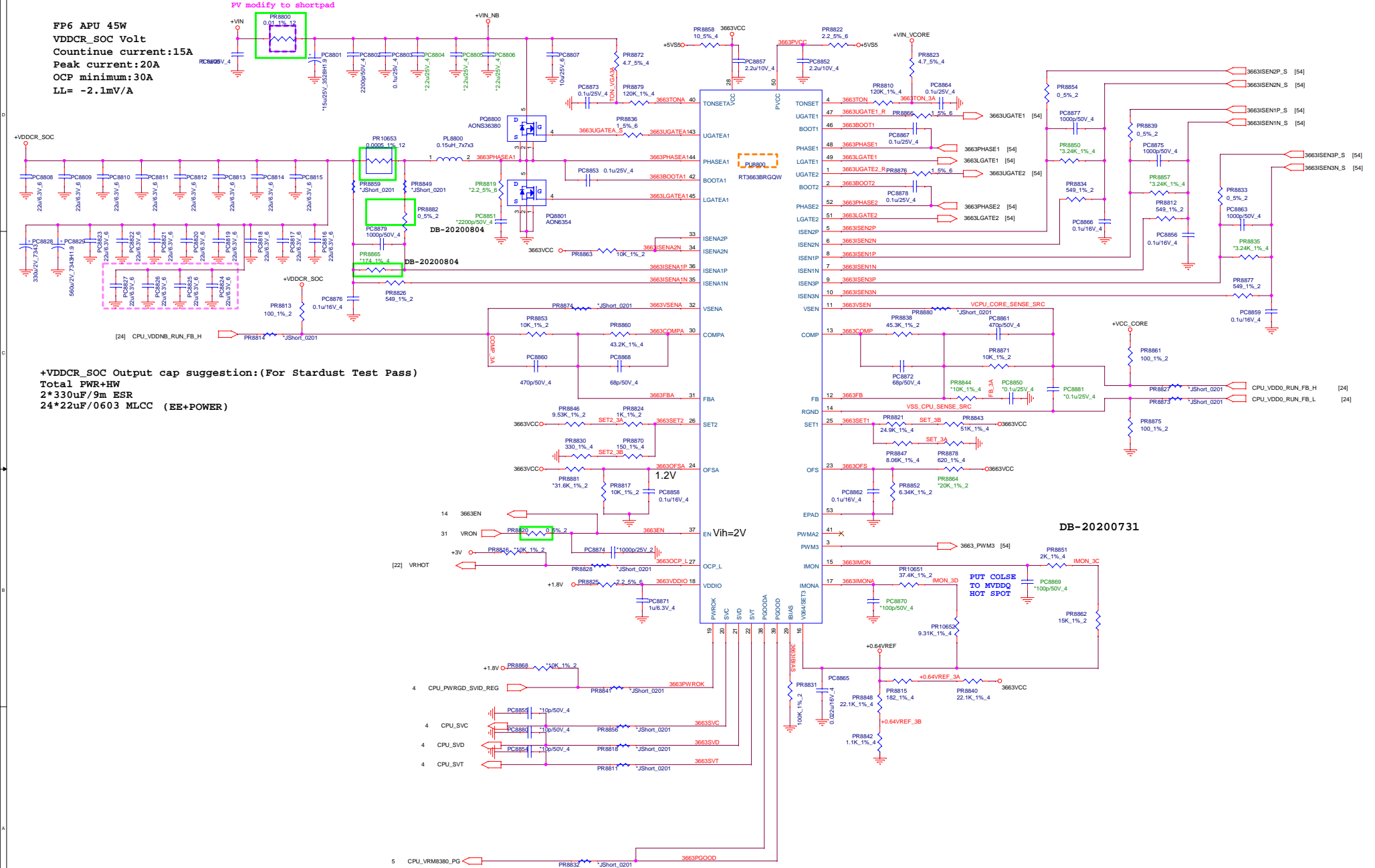


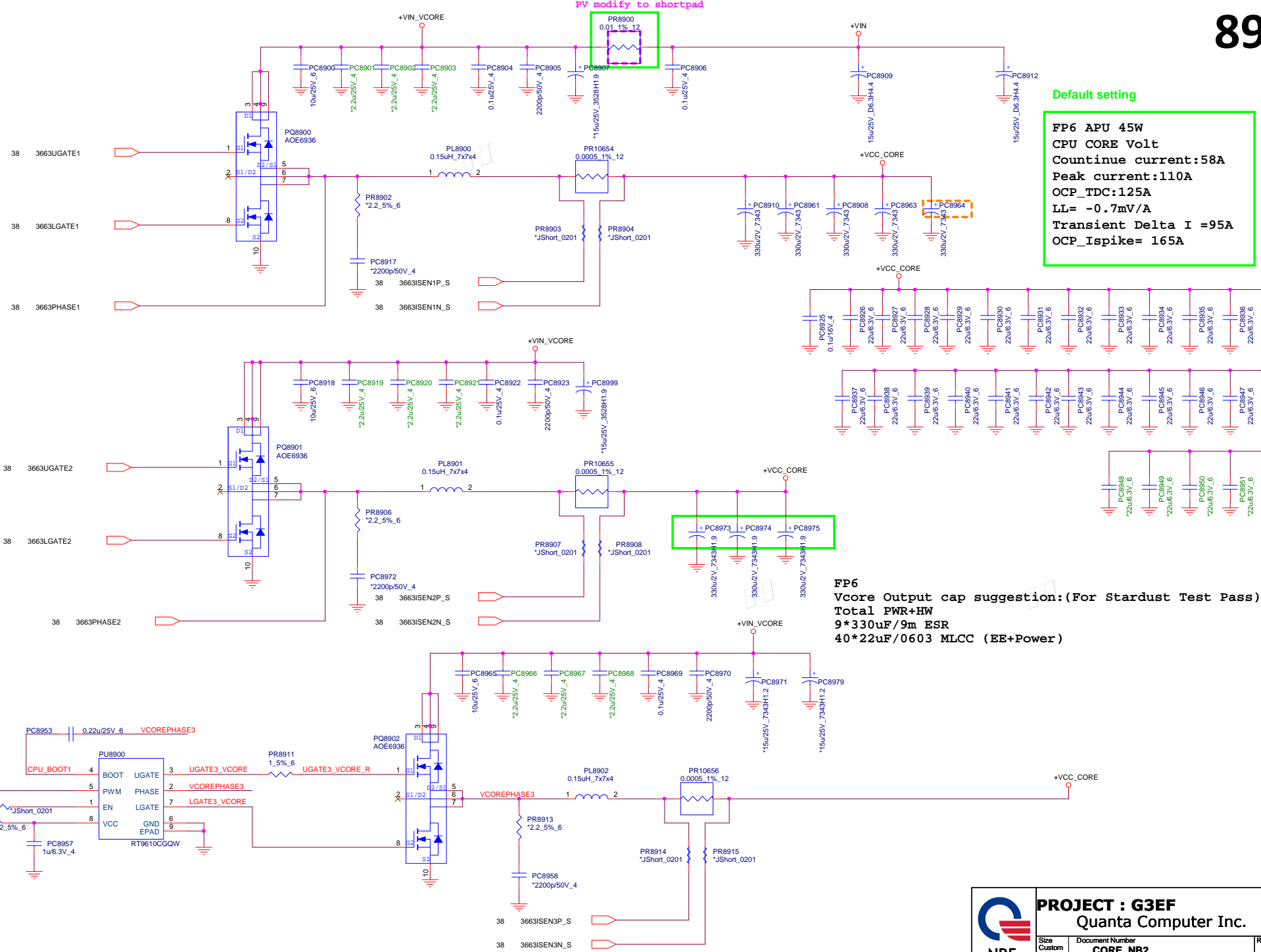
PROJECT : G3EF
Quanta Computer Inc.

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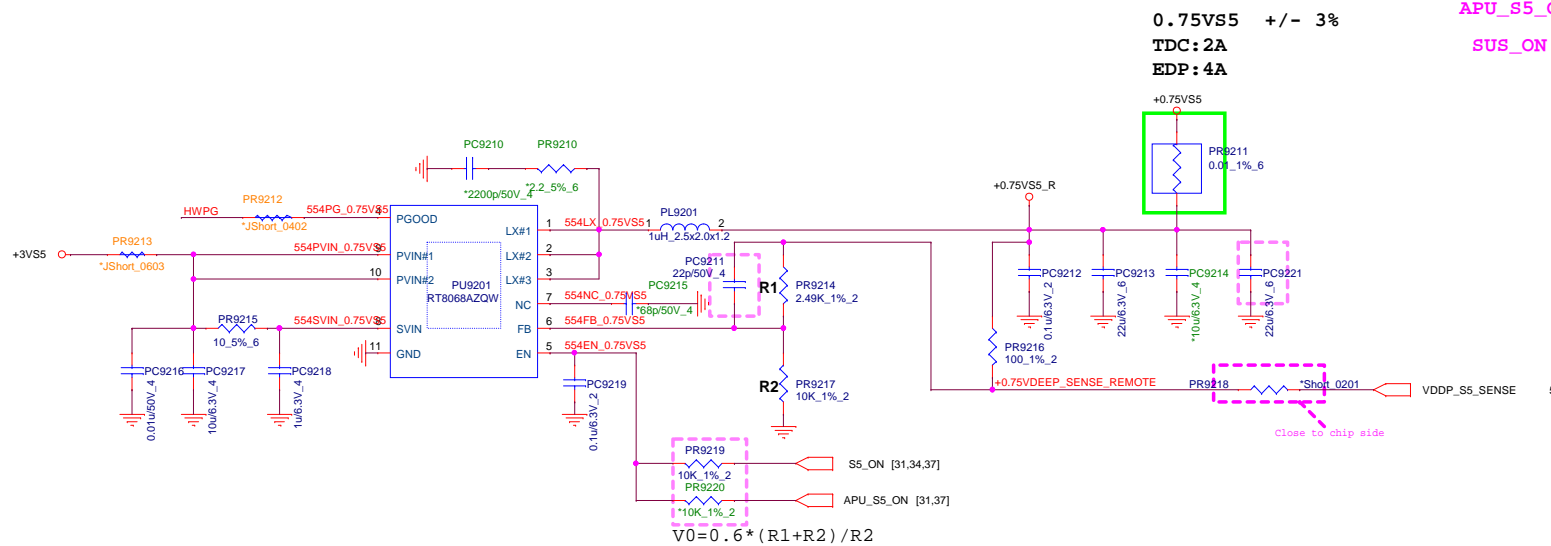
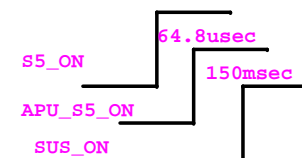
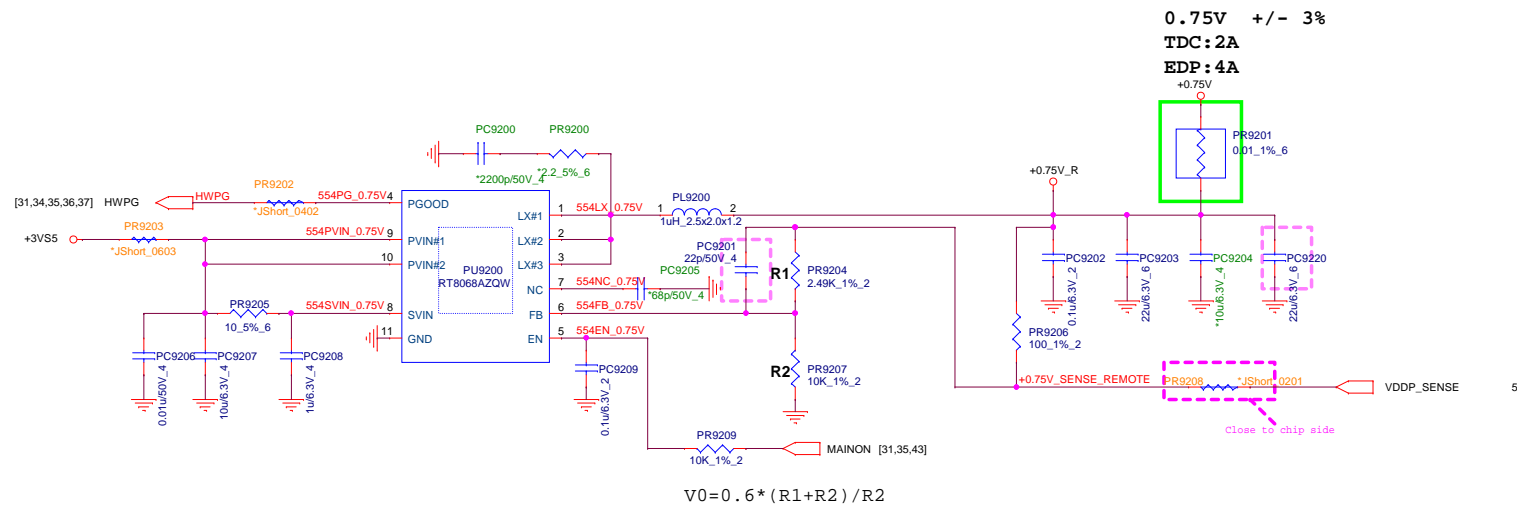
```
FP6 APU 45W
VDDCR_SOC Volt
Countinue current:15A
Peak current:20A
OCP minimum:30A
LL= -2.1mV/A
```

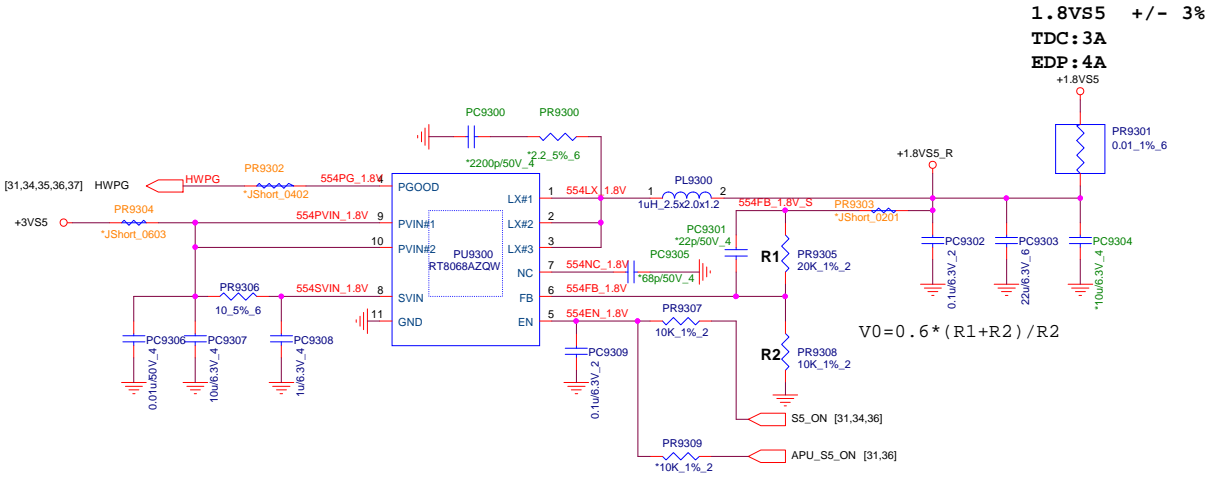




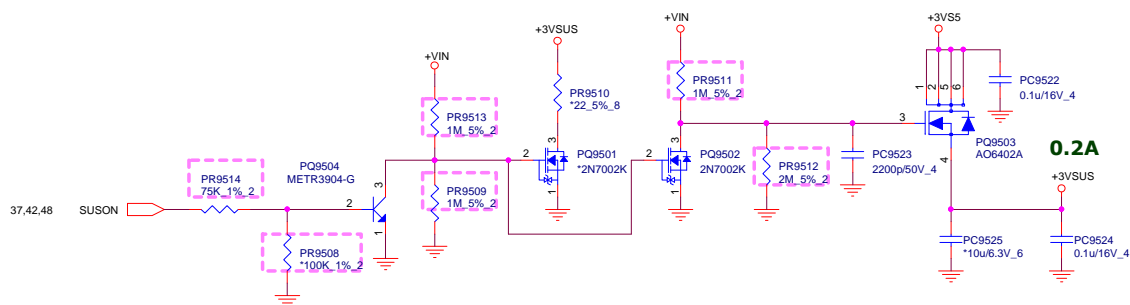
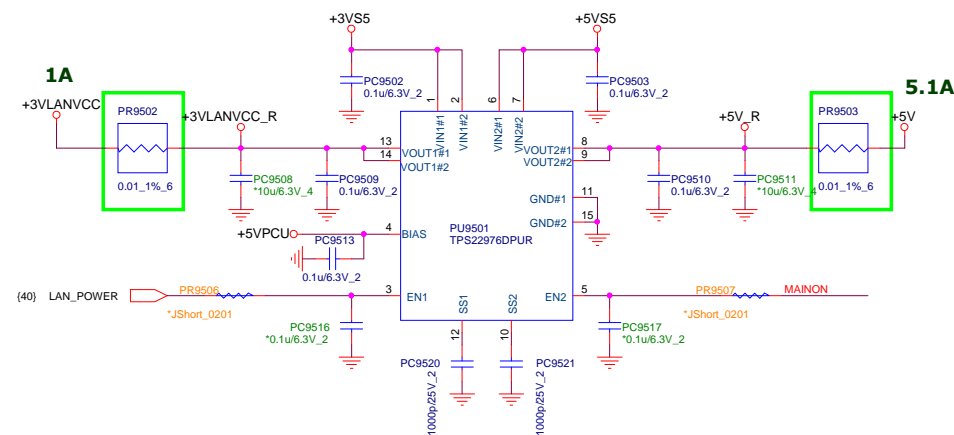
NA

NA



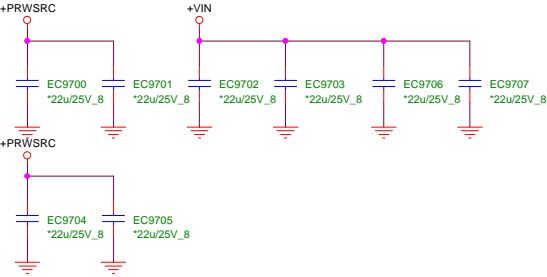


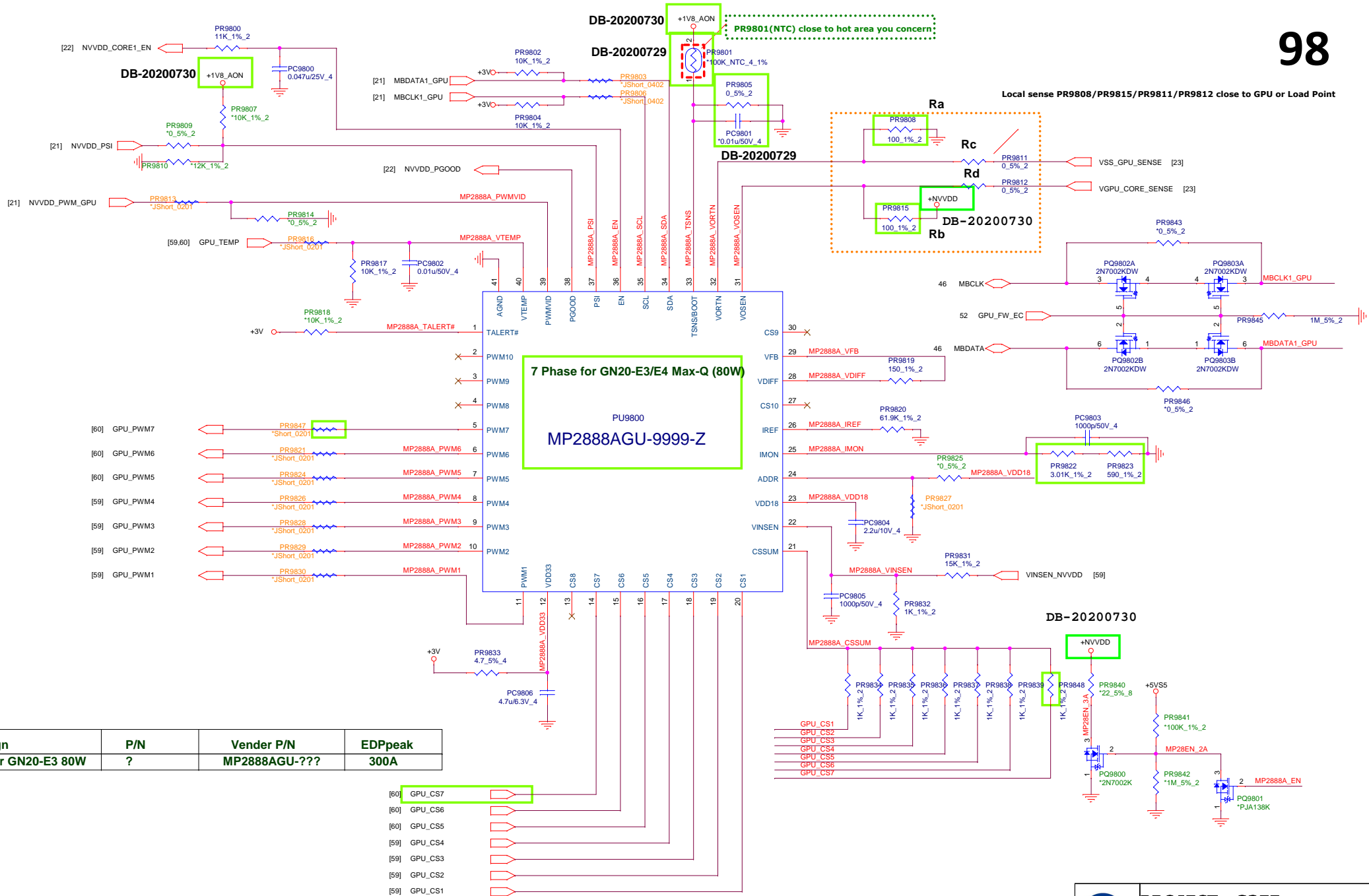
NA



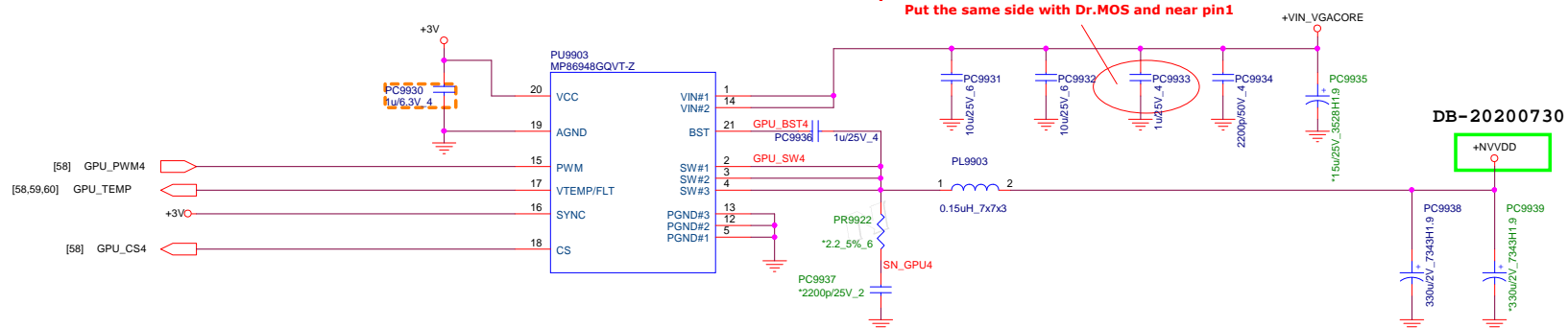
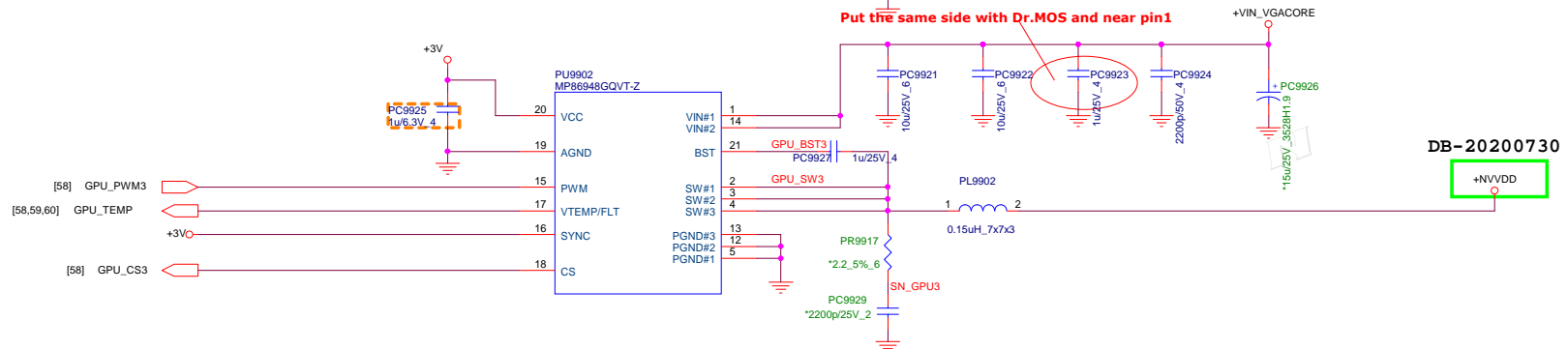
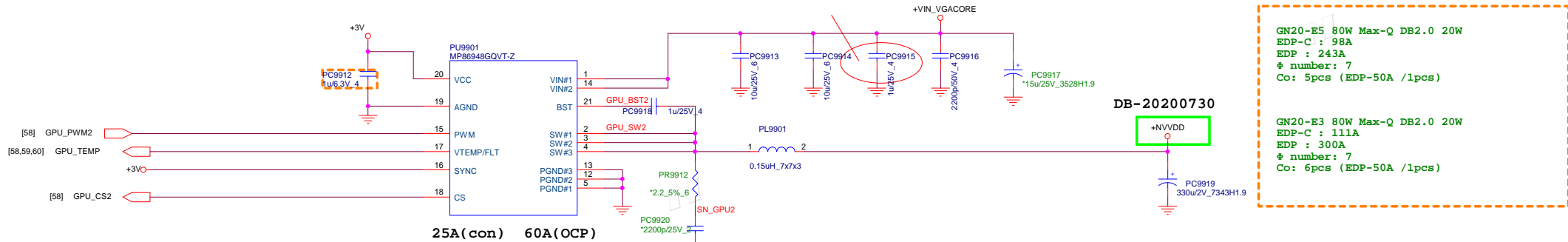
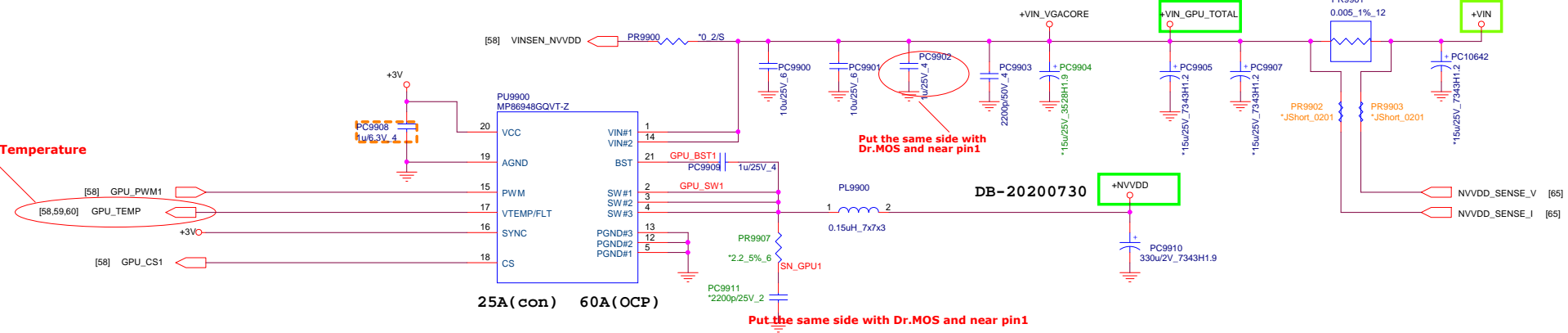
NA

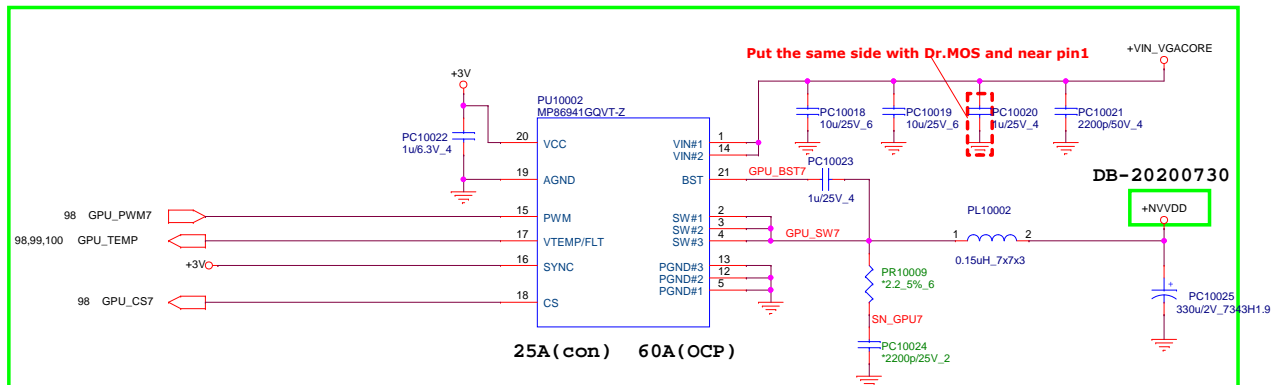
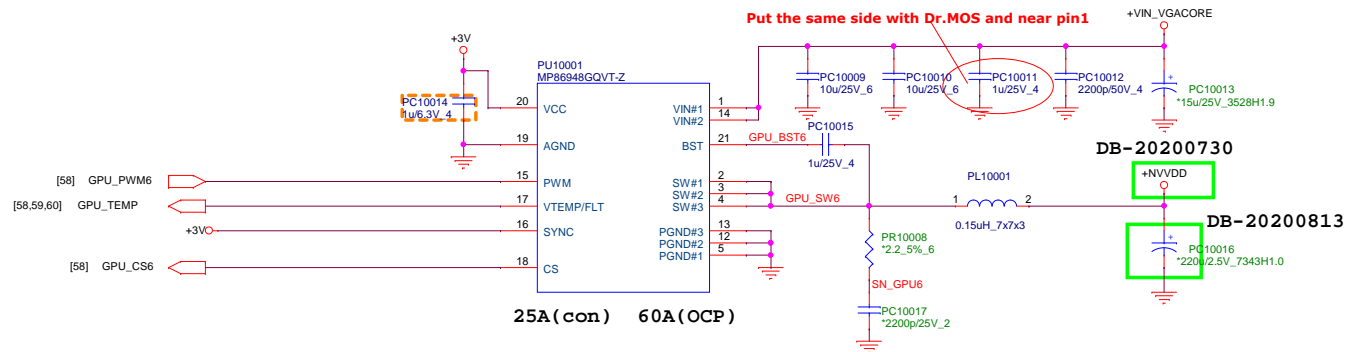
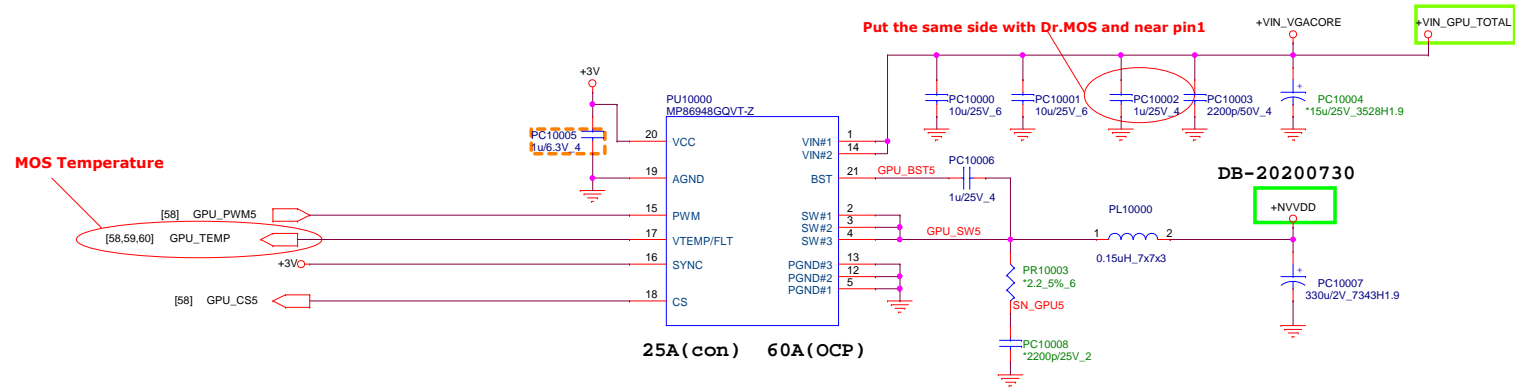
Reserve for ISEN

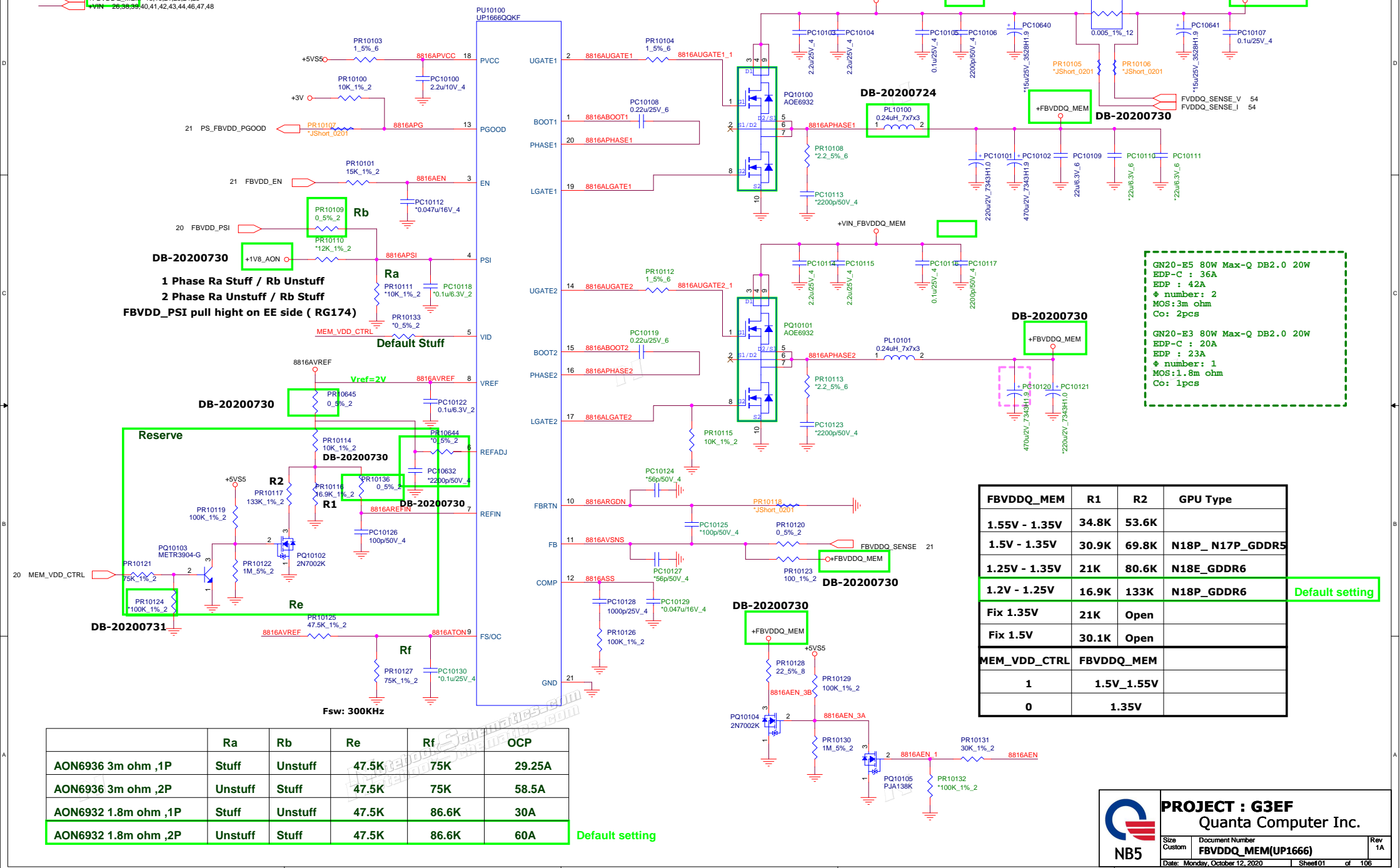




MOS Temperature





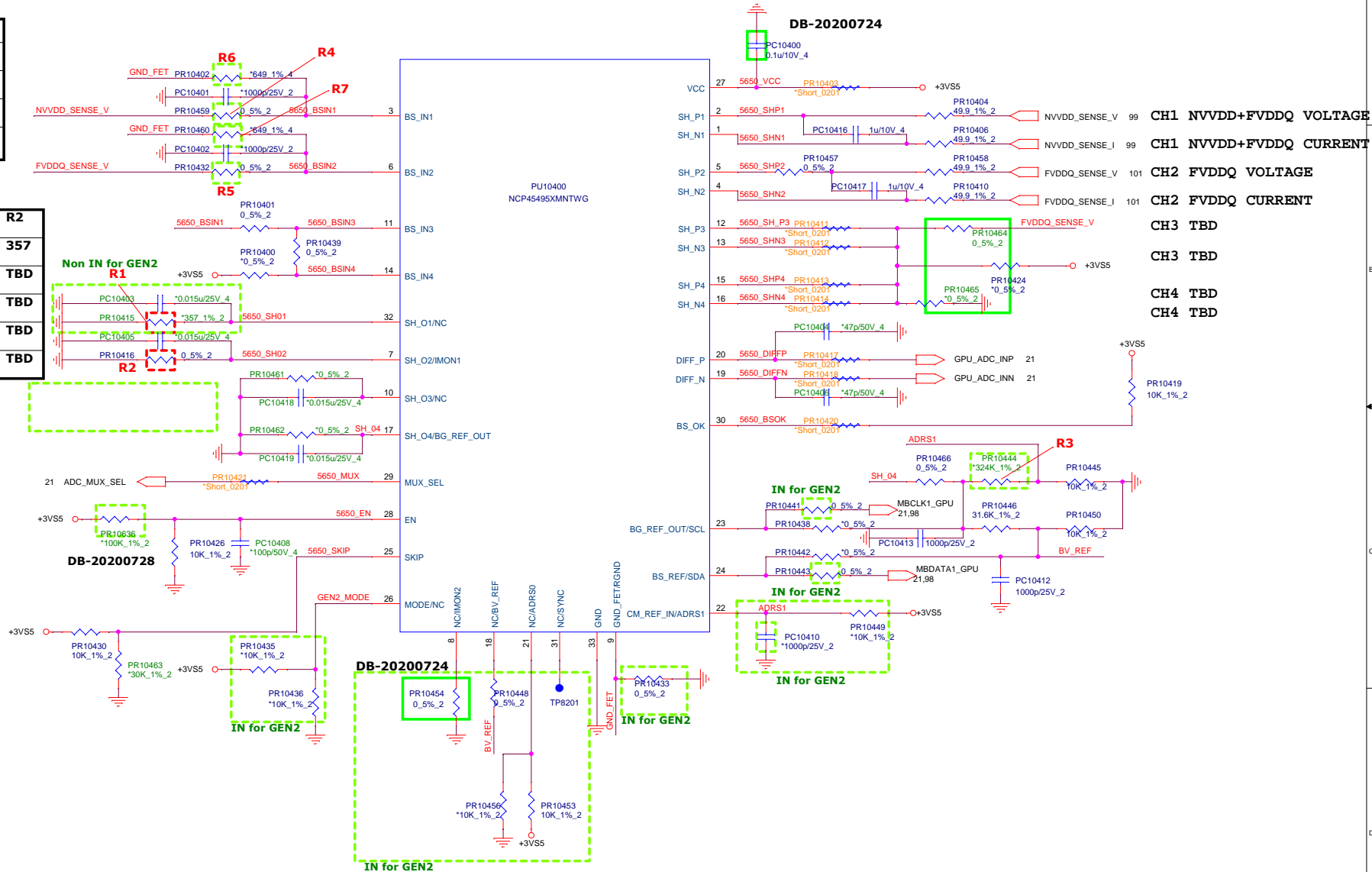


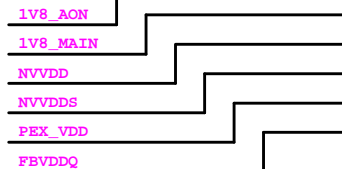
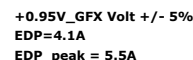
NA

NA

GEN1	UPI	OnSemi
R1, R2	357	475
R3	324K	243K
R4, R5	75K	75K
R6, R7	487	649

UPI OVR Setting	R1	R2
QN20-P1	357	357
QN20-P1 Max-Q	TBD	TBD
GN20-P0	TBD	TBD
GN20-E7	TBD	TBD
GN20-E3/E4/E5	TBD	TBD
GN20-E3/E4/E5/E7 Max-Q	TBD	TBD





37 DC_PROCHOT_OFF

37.4155 ACIN

DC_PROCHOT_OFF

ACIN

PQ10603A *2N7002KDW

PQ10603B *2N7002KDW

PQ10604A *2N7002KDW

PQ10604B *2N7002KDW

PR10538 *10K_1%_2

PR10539 *10K_1%_2

PR10540 *10K_1%_2

PR10541 *10K_1%_2

4.375 H_PROCHOT#

DGPU_PROCHOT_EC# 20.3755

3V3

HW/PRHOT1

